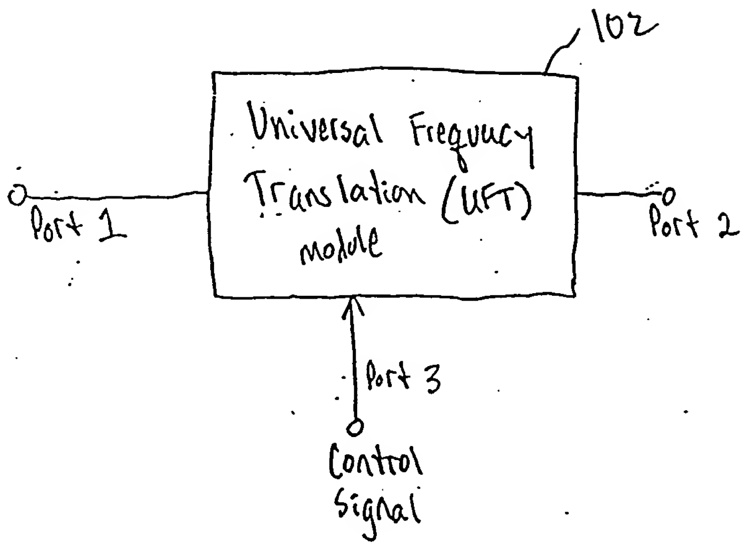

102
Universal Frequency Translation (UFT) module
Port 1
Port 2
Port 3
Control Signal

FIG. 1A

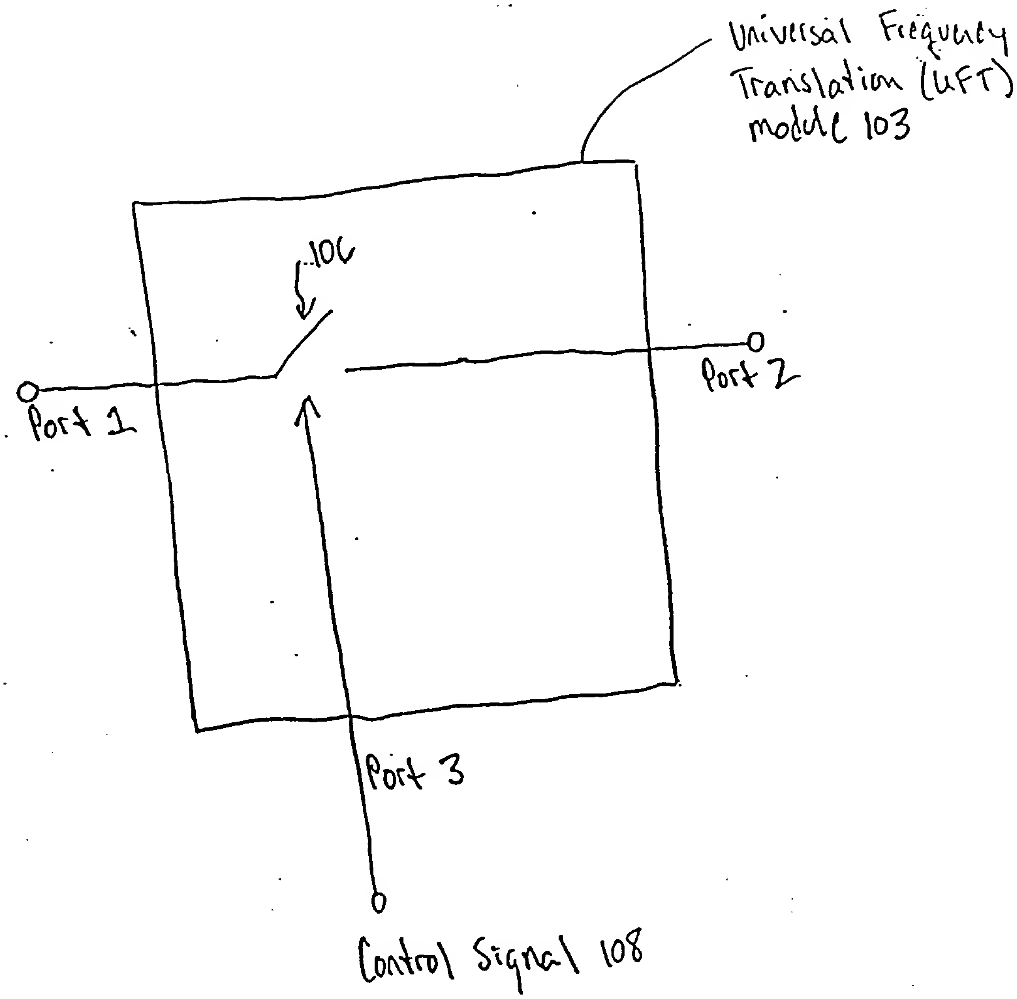

Universal Frequency Translation (UFT) module 103
106
Port 1
Port 2
Port 3
Control Signal 108

FIG. 1B

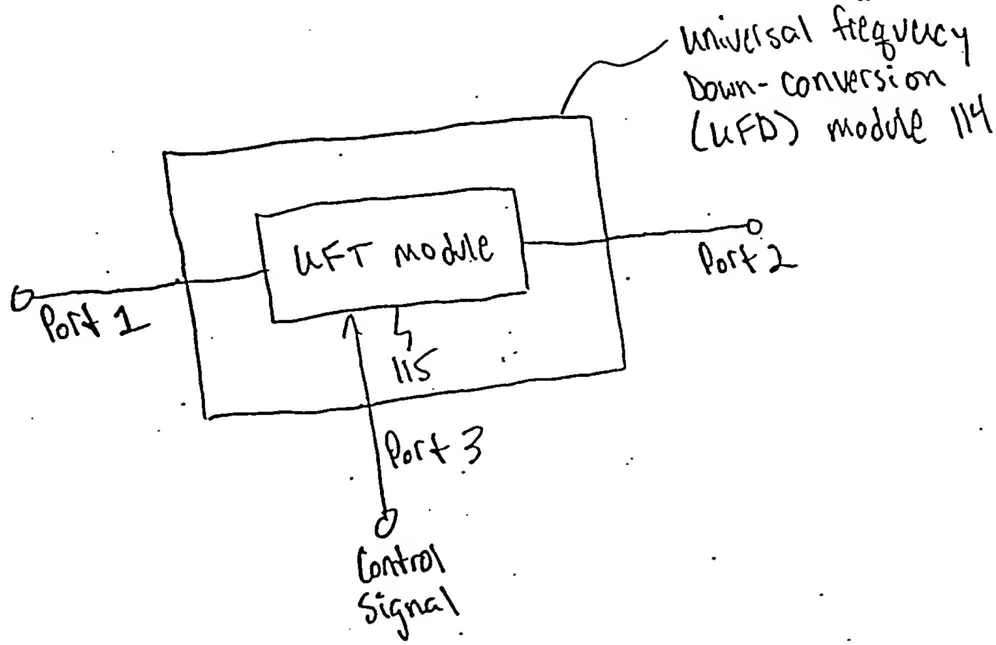

Universal frequency
Down-conversion
(UFD) module 114
UFT module
Port 1
Port 2
115
Port 3
Control
Signal

FIG. 1C

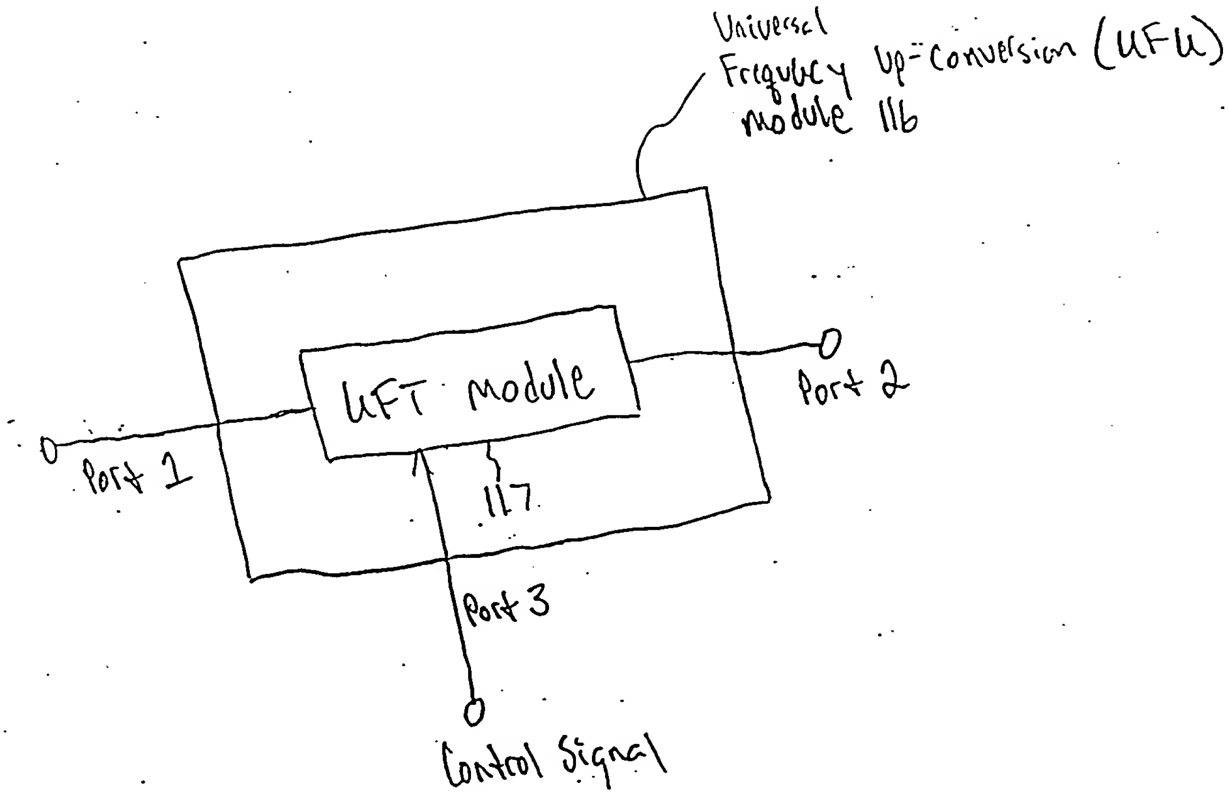

Universal
Frequency Up-Conversion (UFU)
module 116
UFT Module
Port 1
Port 2
117
Port 3
Control Signal

FIG. 1D

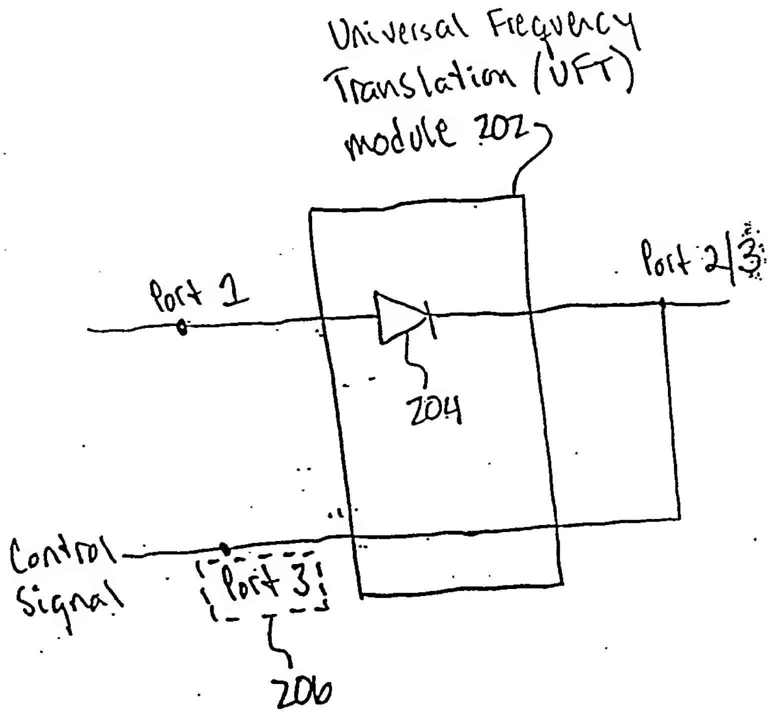

Universal Frequency Translation (UFT) module 202
Port 1
204
Port 2/3
Control Signal
Port 3
206

FIG. 2A

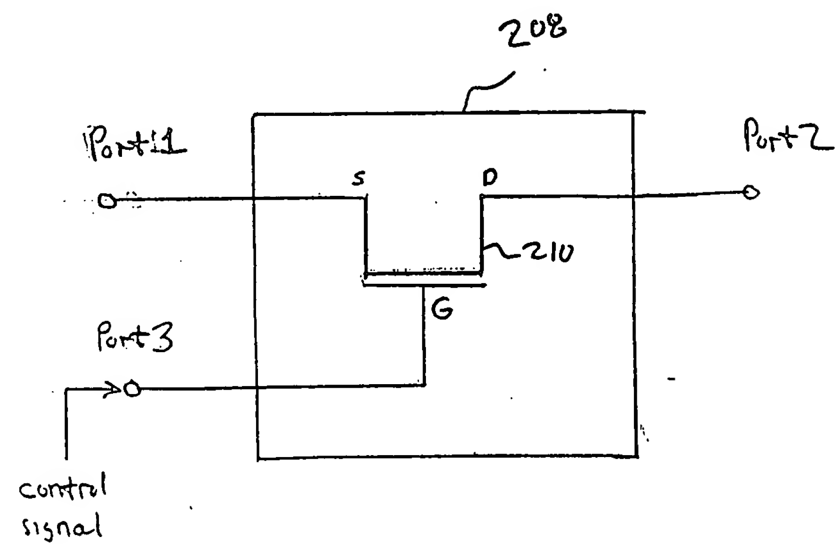


Fig. 2B

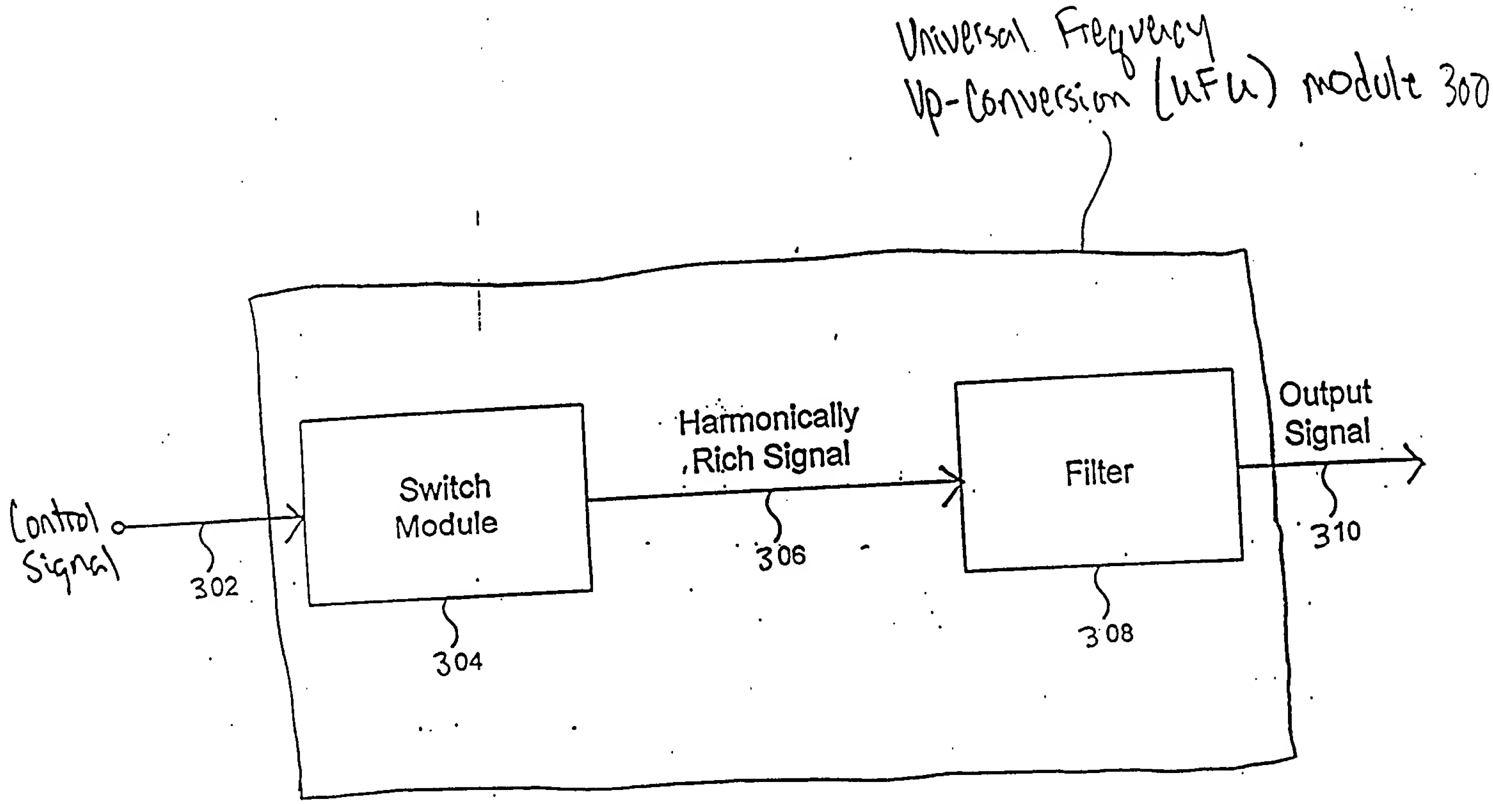

Universal Frequency
Up-Conversion (UFU) module 300
Control Signal
302
Switch Module
304
Harmonically Rich Signal
306
Filter
308
Output Signal
310

FIG. 3

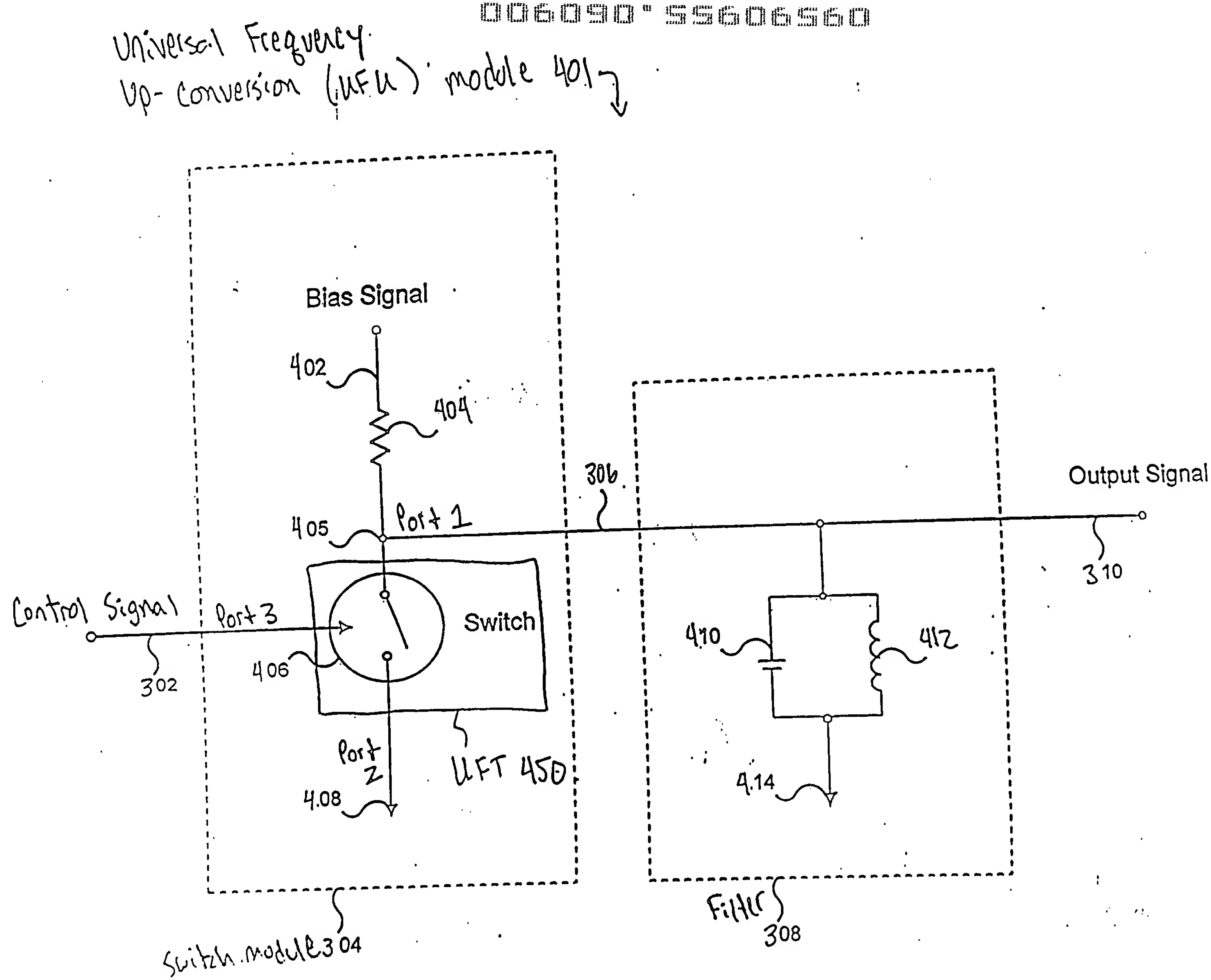


FIG. 4

9809-02.vsd/47

3

00609055 .060900

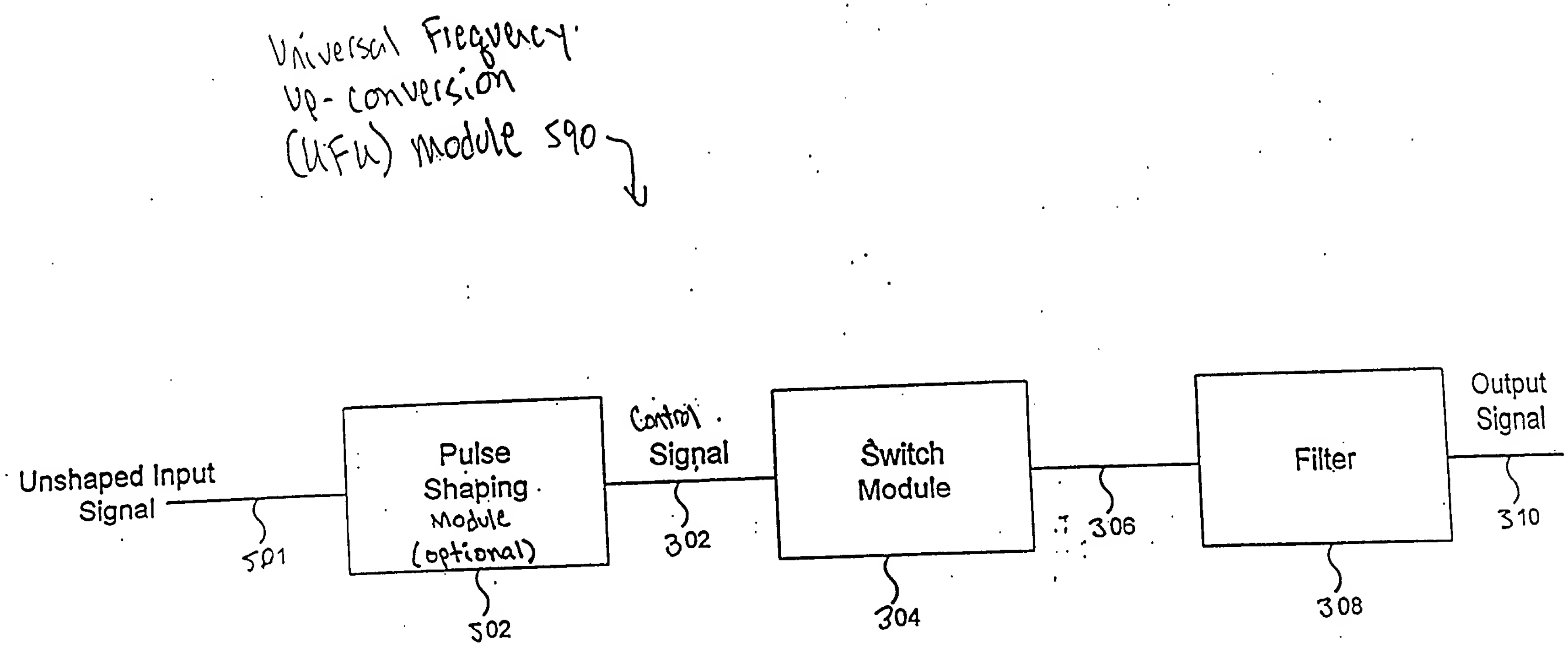


FIG. 5

9809-02.vsd/48

006090"55606560

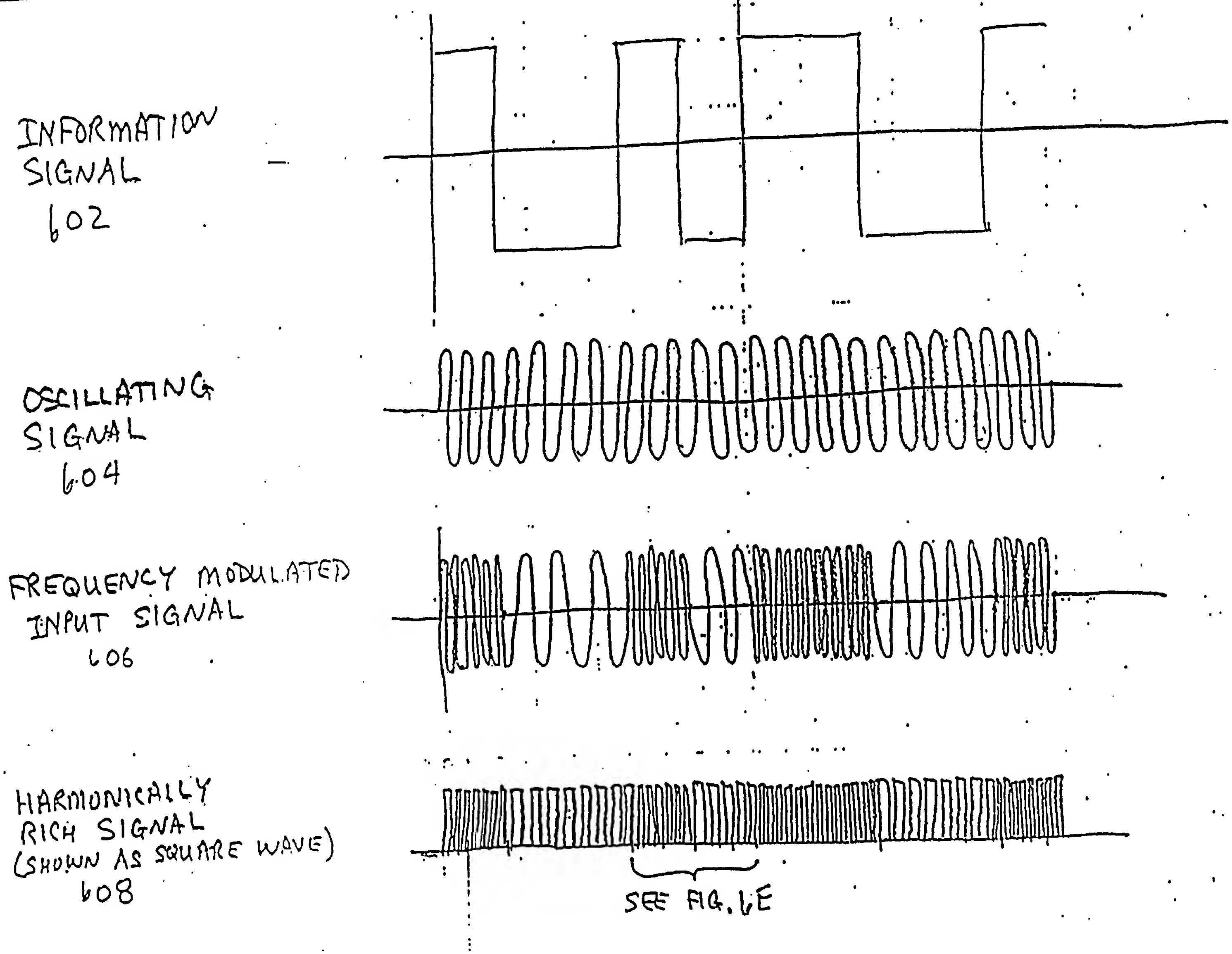


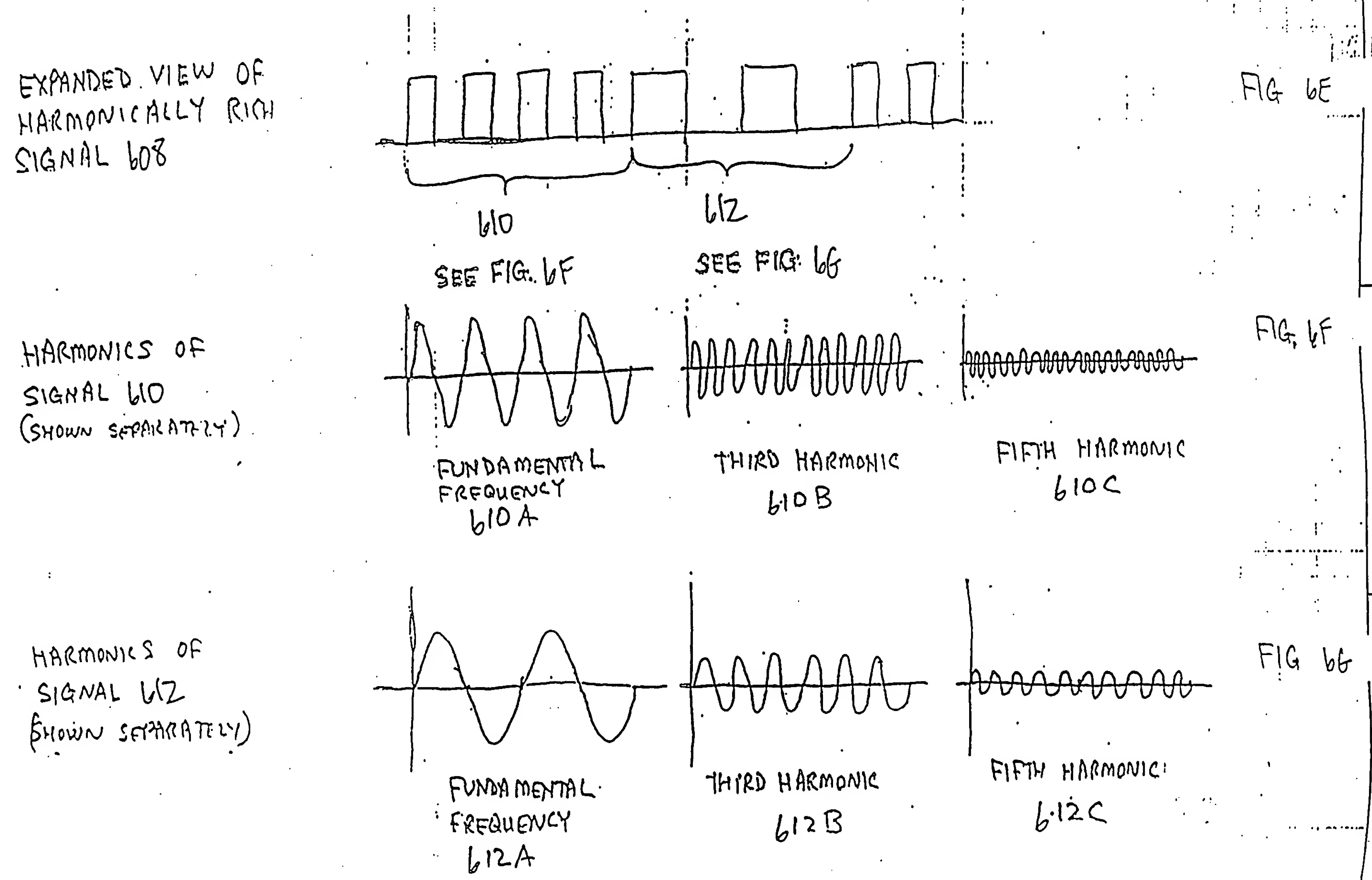
FIG. 6A

FIG. 6B

FIG. 6C

FIG. 6D

FIG. 6



EXPANDED VIEW OF HARMONICALLY RICH SIGNAL 608
610
612
SEE FIG. 6F
SEE FIG. 6G
HARMONICS OF SIGNAL 610 (SHOWN SEPARATELY)
FUNDAMENTAL FREQUENCY 610A
THIRD HARMONIC 610B
FIFTH HARMONIC 610C
HARMONICS OF SIGNAL 612 (SHOWN SEPARATELY)
FUNDAMENTAL FREQUENCY 612A
THIRD HARMONIC 612B
FIFTH HARMONIC 612C
FIG 6E
FIG. 6F
FIG 6G

FIG. 6 (cont)

3

00609O"55606560

HARMONICS OF SIGNALS 610 AND 612 (SHOWN SIMULTANEOUSLY BUT NOT SUMMED)

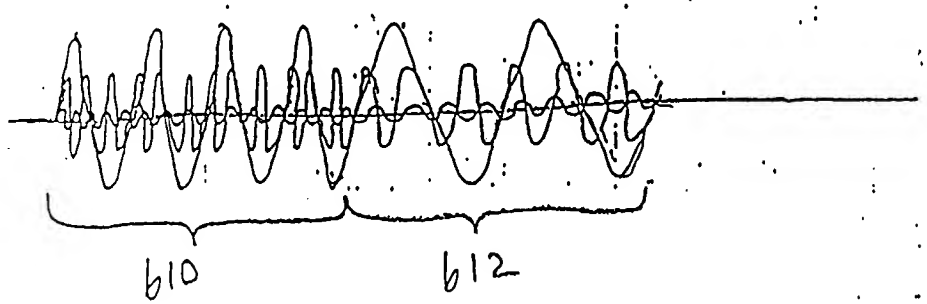


FIG 6H

FILTERED OUTPUT SIGNAL 614

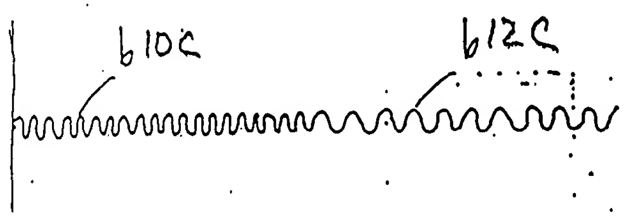


FIG. 6I

FIG 6 (cont.)

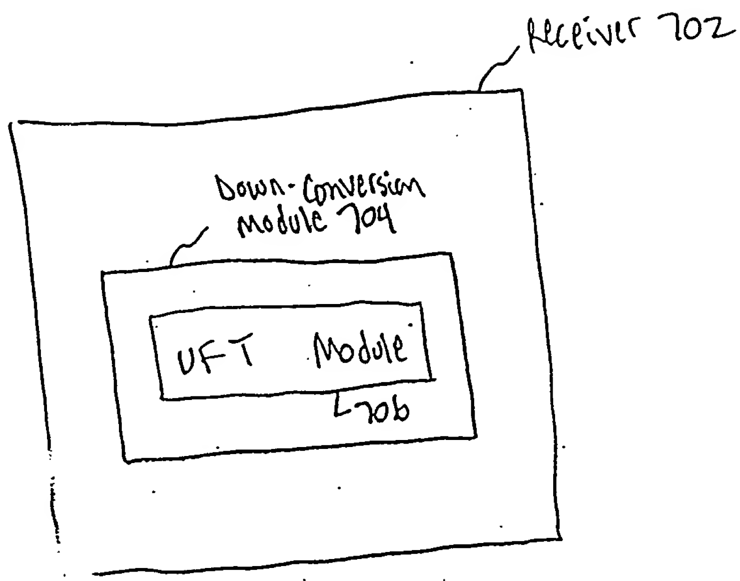


FIG. 7

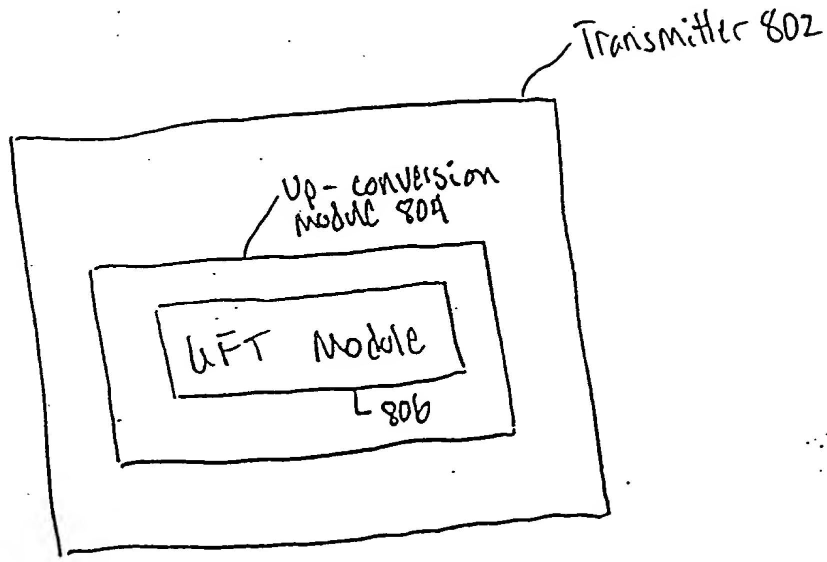


FIG. 8

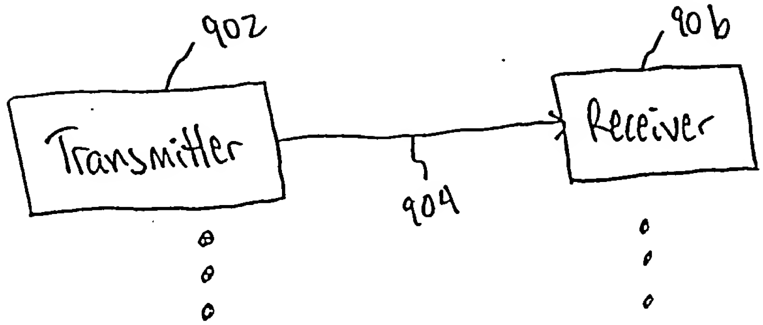
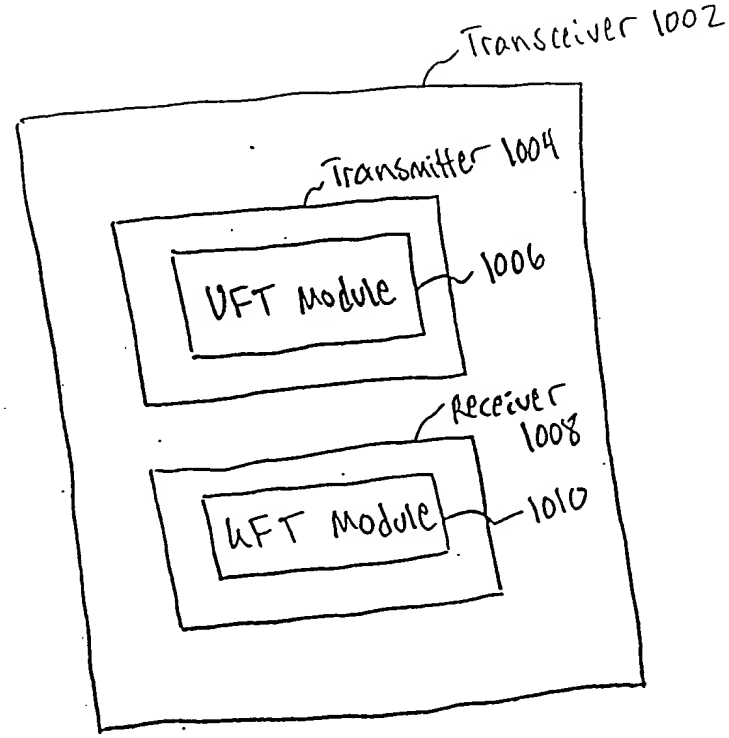


FIG. 9



Transceiver 1002
Transmitter 1004
UFT Module
1006
Receiver
1008
UFT Module
1010

FIG. 10

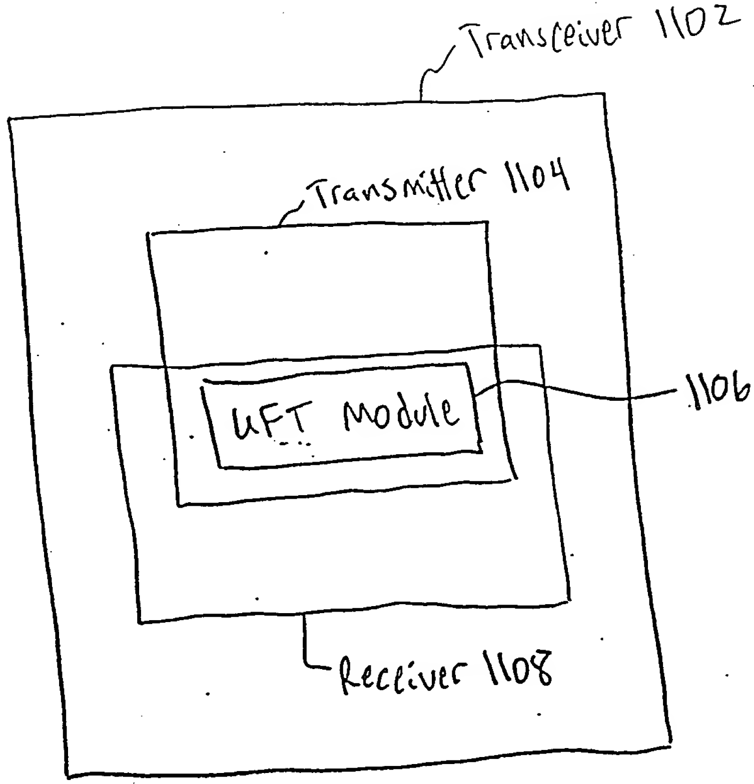

Transceiver 1102
Transmitter 1104
UFT Module
1106
Receiver 1108

FIG. 11

m

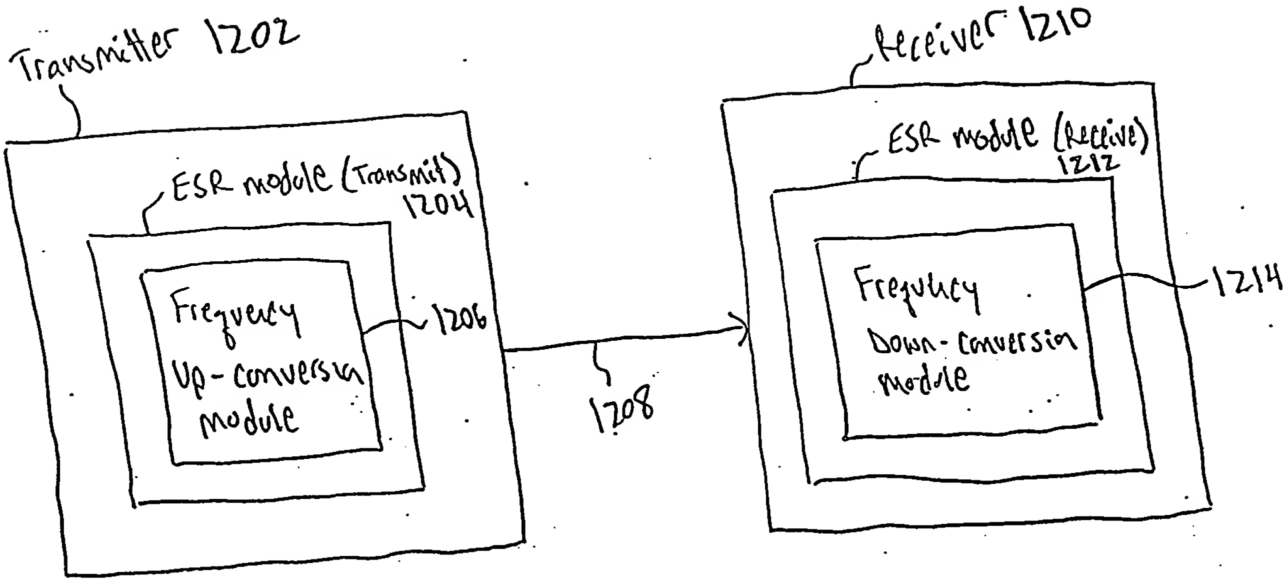

Transmitter 1202
ESR module (Transmit) 1204
Frequency Up-conversion module
1206
1208
Receiver 1210
ESR module (Receive) 1212
Frequency Down-conversion module
1214

FIG. 12

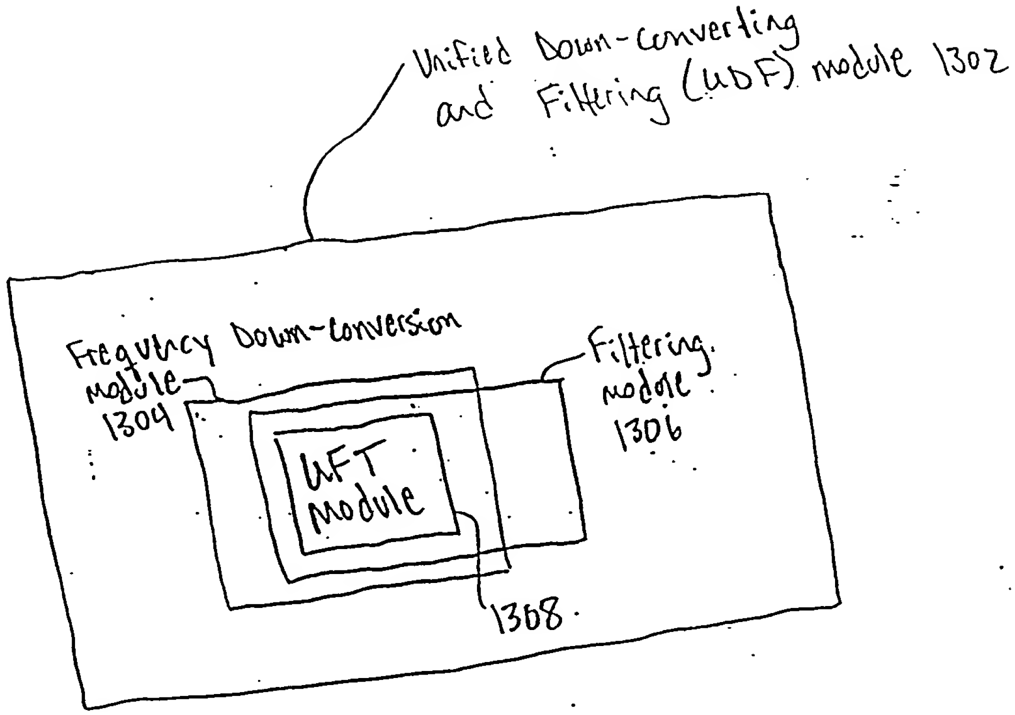

Unified Down-converting and Filtering (UDF) module 1302
Frequency Down-conversion module 1304
Filtering module 1306
UFT Module
1308

FIG. 13

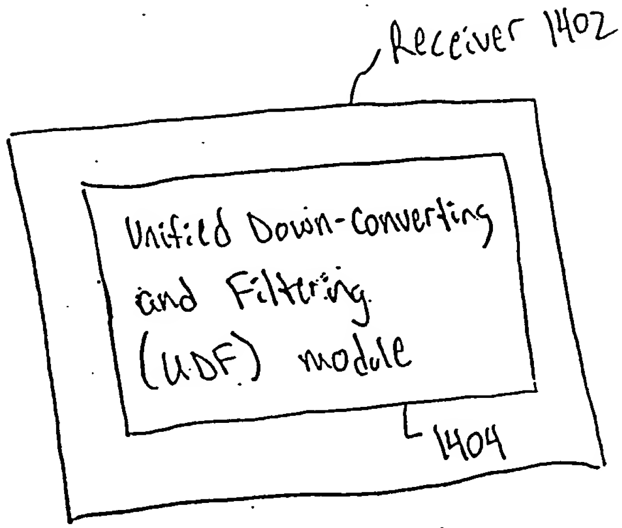

Receiver 1402
Unified Down-Converting
and Filtering
(UDF) module
1404

FIG. 14

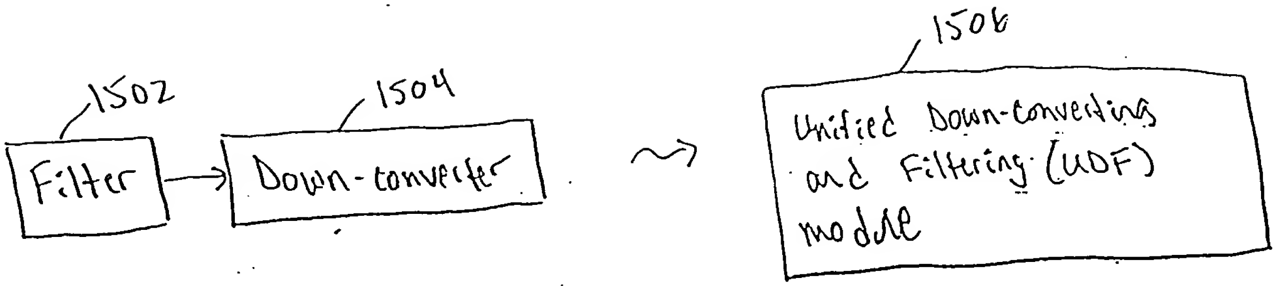


FIG. 15A

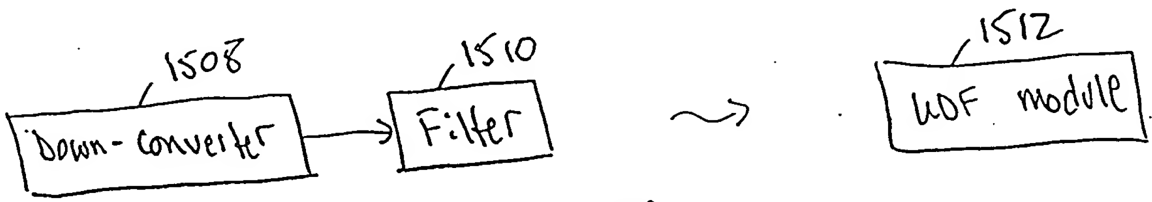


FIG. 15B

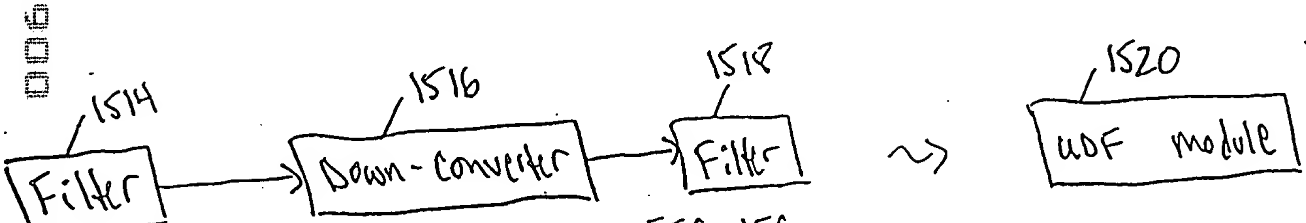


FIG. 15C

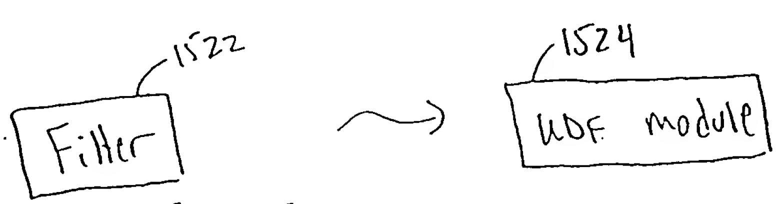


FIG. 15D

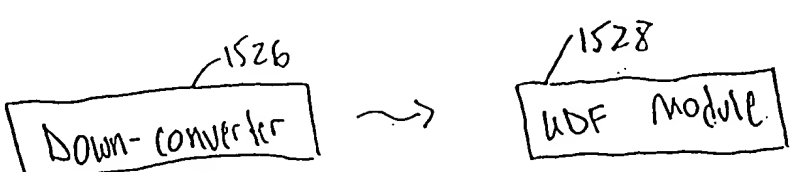


FIG. 15E

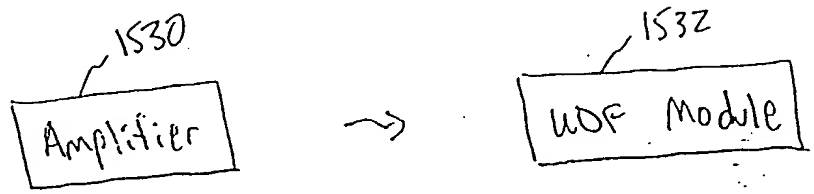


FIG. 15F

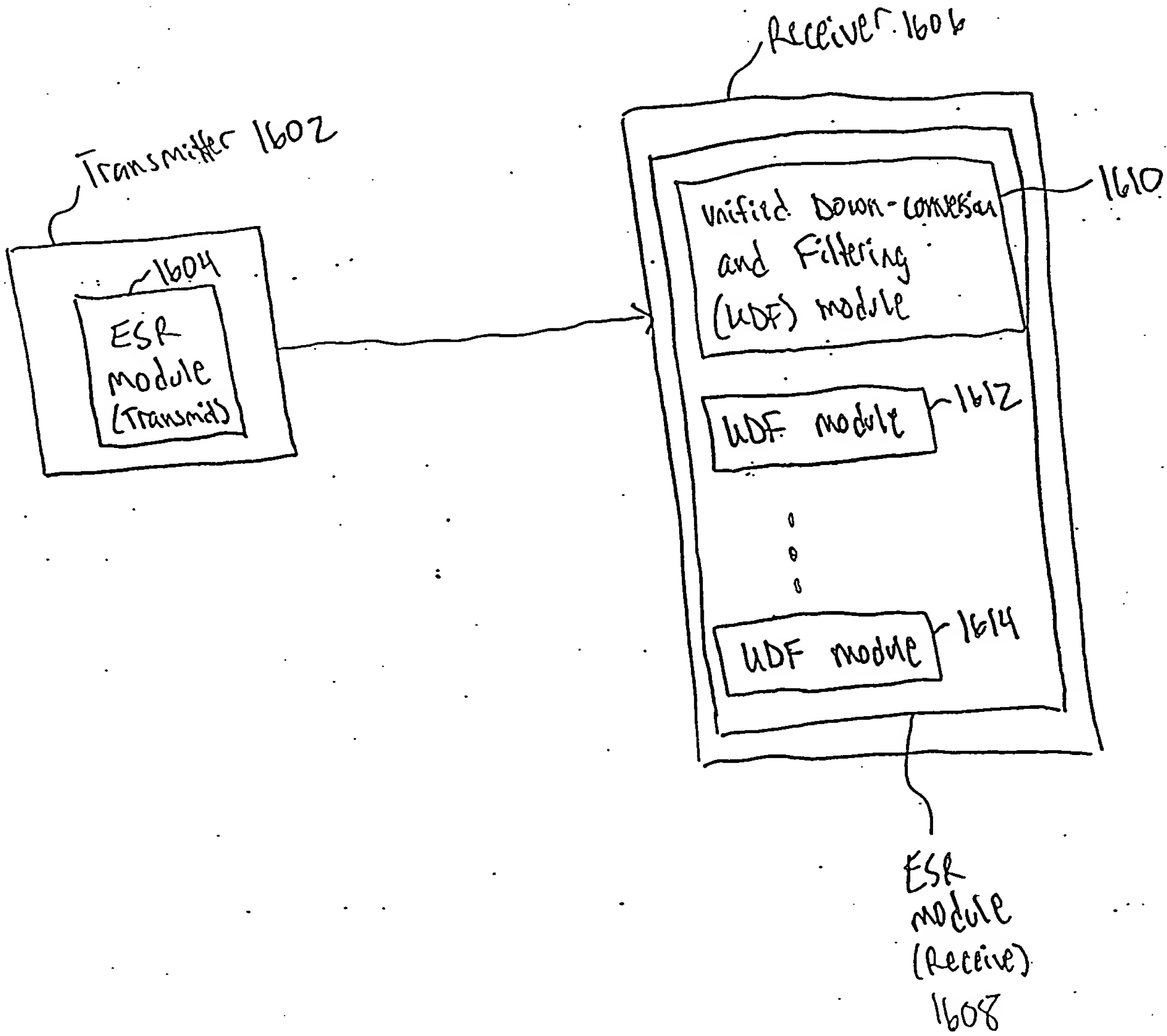

Transmitter 1602
1604
ESR module (Transmit)
Receiver 1606
Unified Down-conversion and Filtering (UDF) module
1610
UDF module
1612
UDF module
1614
ESR module (Receive) 1608

FIG. 16

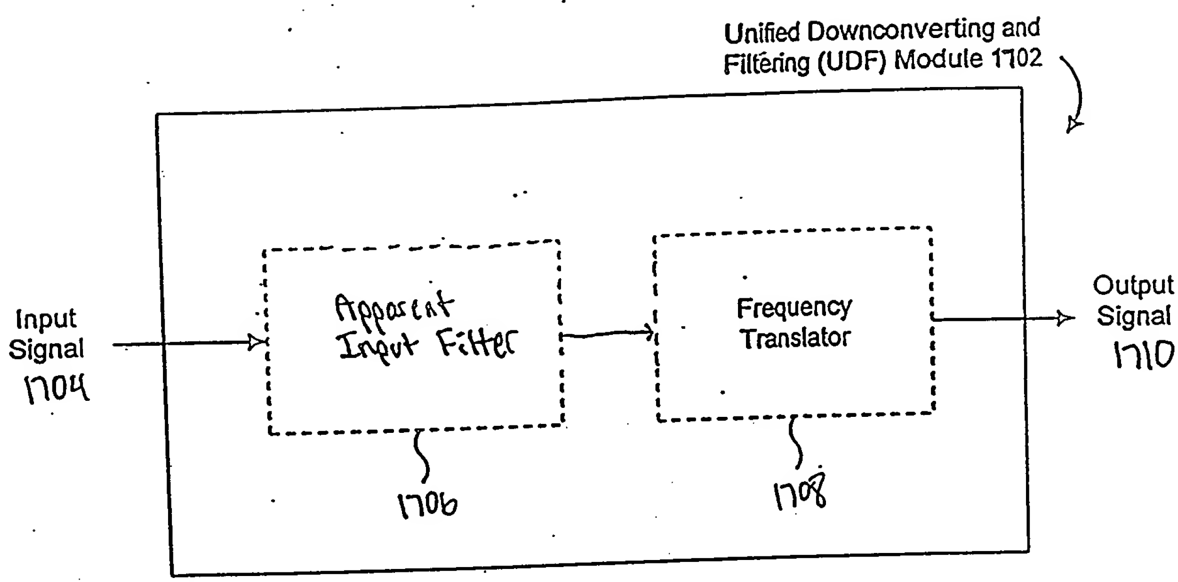

Unified Downconverting and Filtering (UDF) Module 1702
Input Signal 1704
Apparent Input Filter
Frequency Translator
Output Signal 1710
1706
1708

FIG. 17

1802

Time / Node	t-1 (rising edge of ϕ_1)	t-1 (rising edge of ϕ_2)	t (rising edge of ϕ_1)	t (rising edge of ϕ_2)	t+1 (rising edge of ϕ_1)
1902	VI_{t-1} 1804	VI_{t-1} 1808	VI_t 1816	VI_t 1826	VI_{t+1} 1838
1904	—	VI_{t-1} 1810	VI_{t-1} 1818	VI_t 1828	VI_t 1840
1906	VO_{t-1} 1806	VO_{t-1} 1812	VO_t 1820	VO_t 1830	VO_{t+1} 1842
1908	—	VO_{t-1} 1814	VO_{t-1} 1822	VO_t 1832	VO_t 1844
1910	— 1807	—	VO_{t-1} 1824	VO_{t-1} 1834	VO_t 1846
1912	—	— 1815	—	VO_{t-1} 1836	VO_{t-1} 1848
1918	—	—	—	—	VI_t - 0.1 * VO_t - 0.8 * VO_{t-1} 1850

FIG. 18

9809-02.vsd/17

006090" 55606560

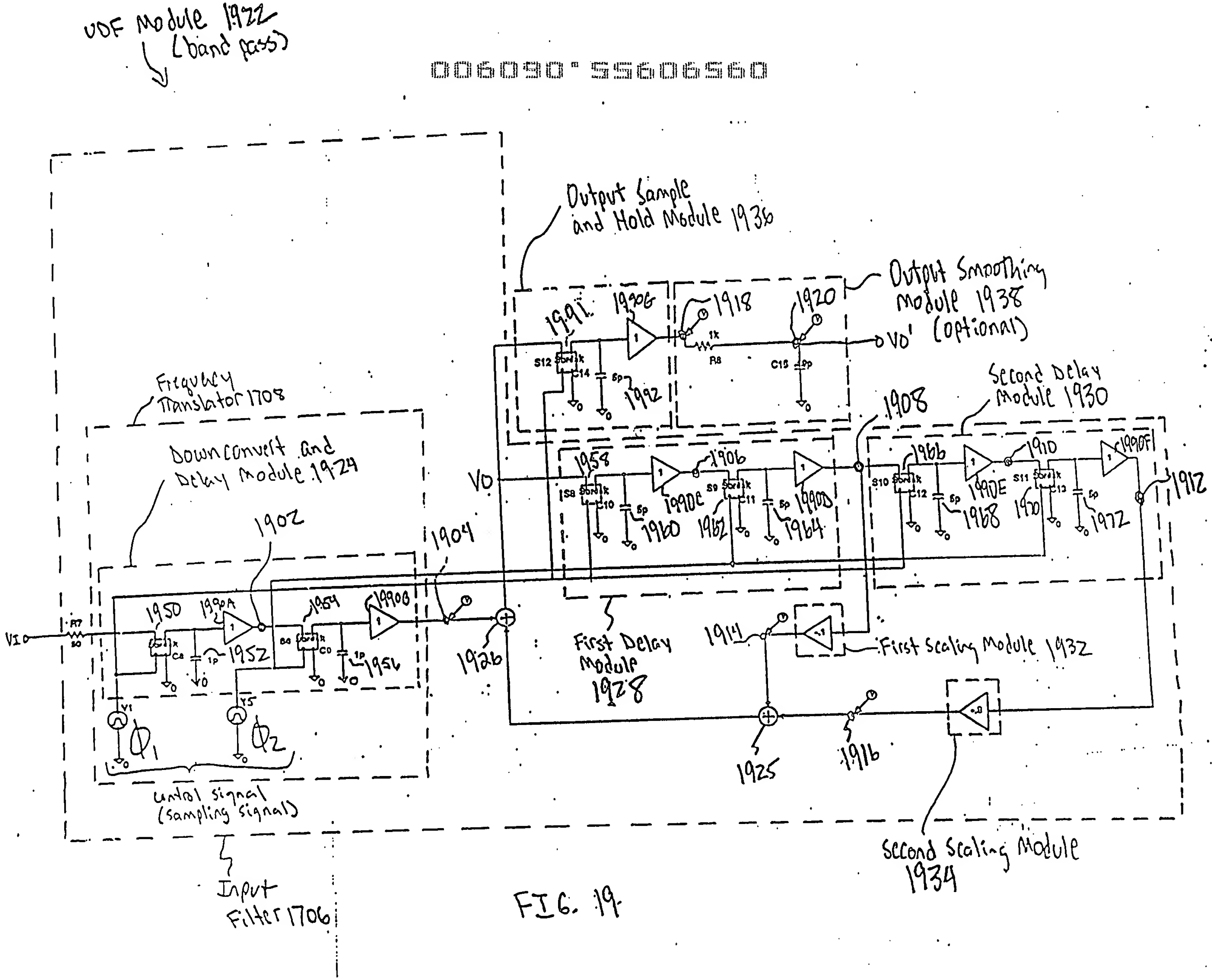


FIG. 19.

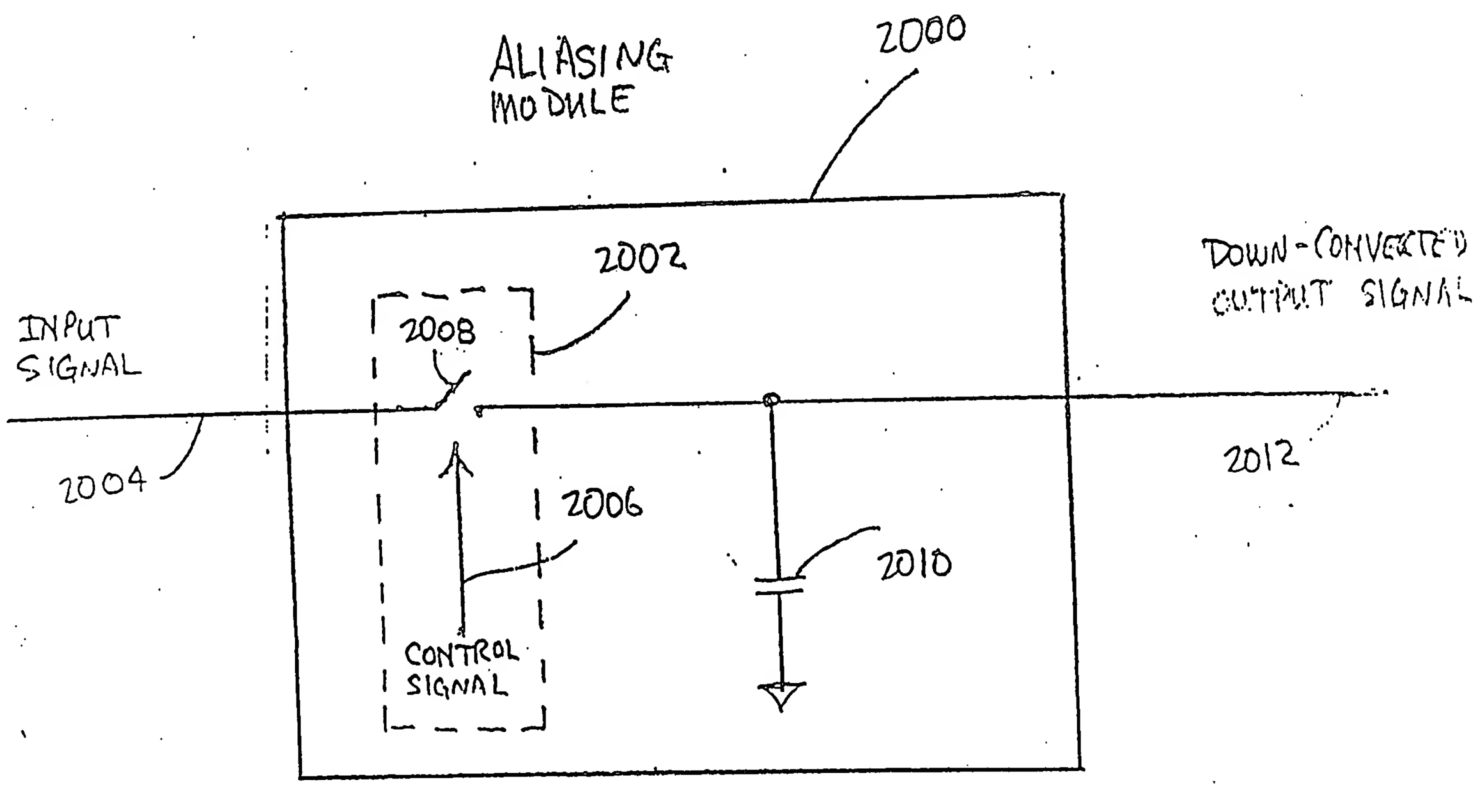

ALIASING MODULE
2000
2002
2008
INPUT SIGNAL
2004
2006
CONTROL SIGNAL
2010
DOWN-CONVERTED OUTPUT SIGNAL
2012

FIG. 20A

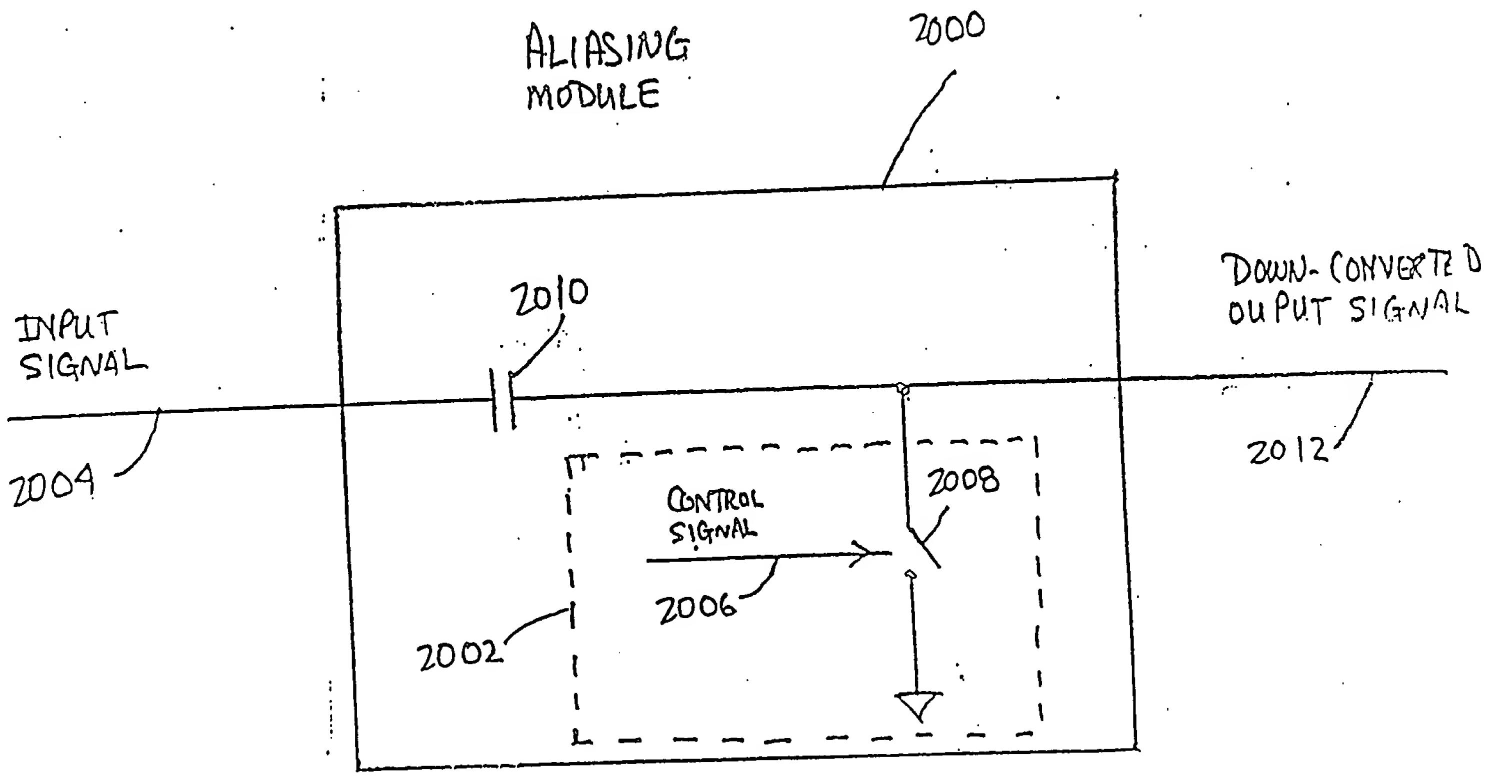

ALIASING
MODULE
2000
INPUT
SIGNAL
2004
2010
DOWN-CONVERTED
OUPUT SIGNAL
2012
CONTROL
SIGNAL
2006
2008
2002

FIG. 20A-1

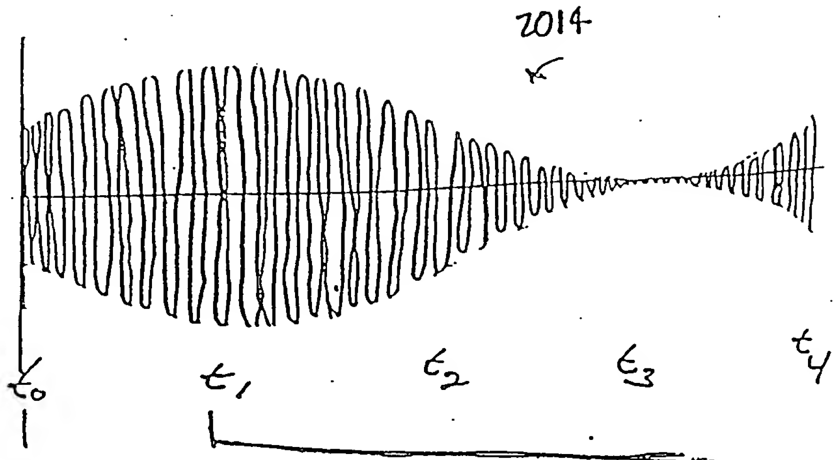


FIG. 20B

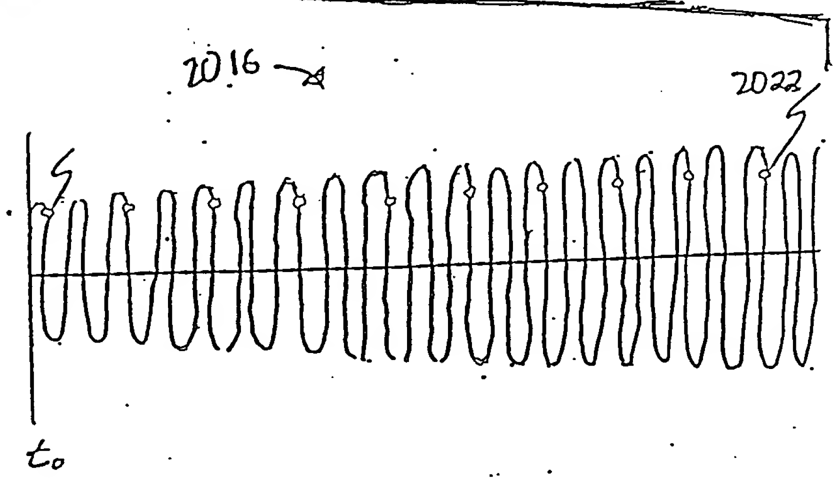


FIG. 20C

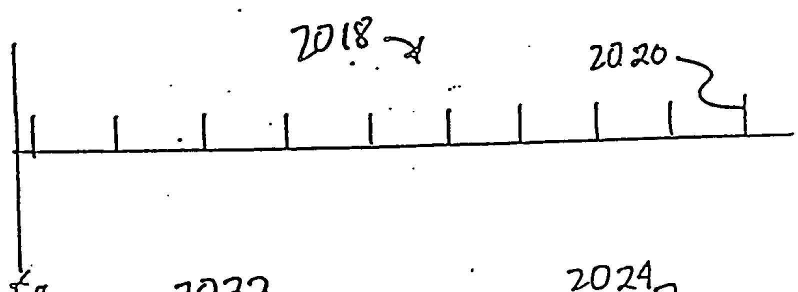


FIG. 20D

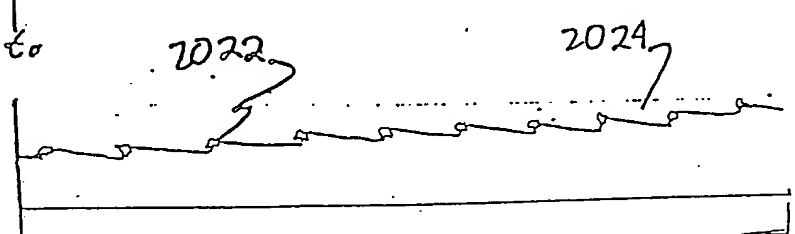


FIG. 20E

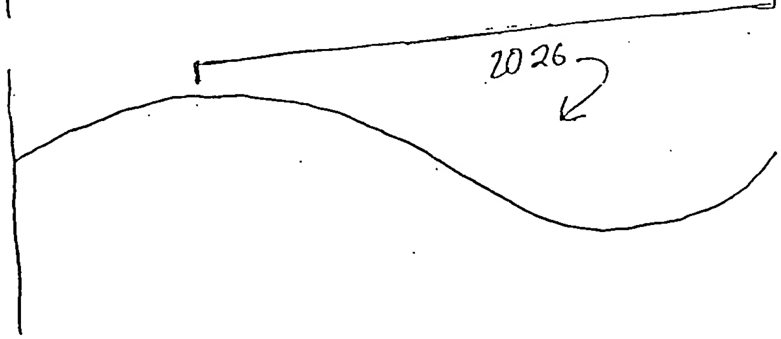


FIG. 20F

09590655.060900

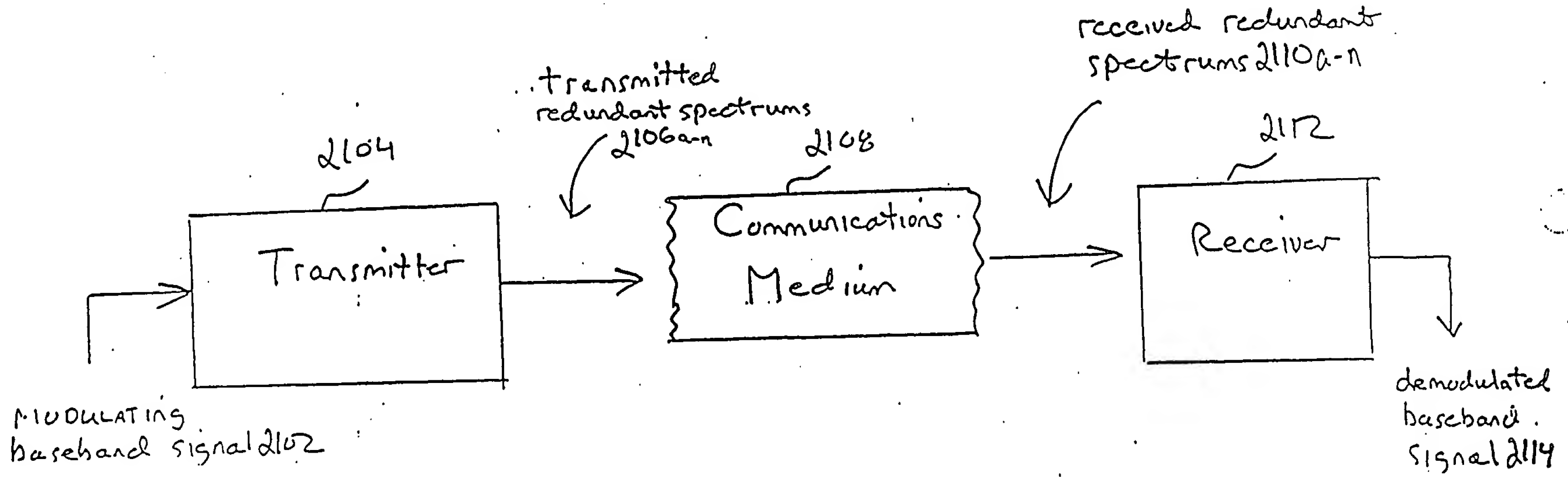


FIG. 21

FIG. 22A

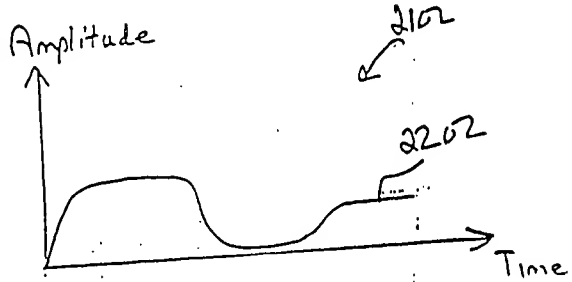


FIG. 22B

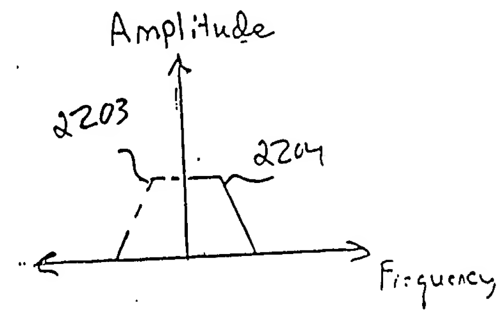


FIG. 22C

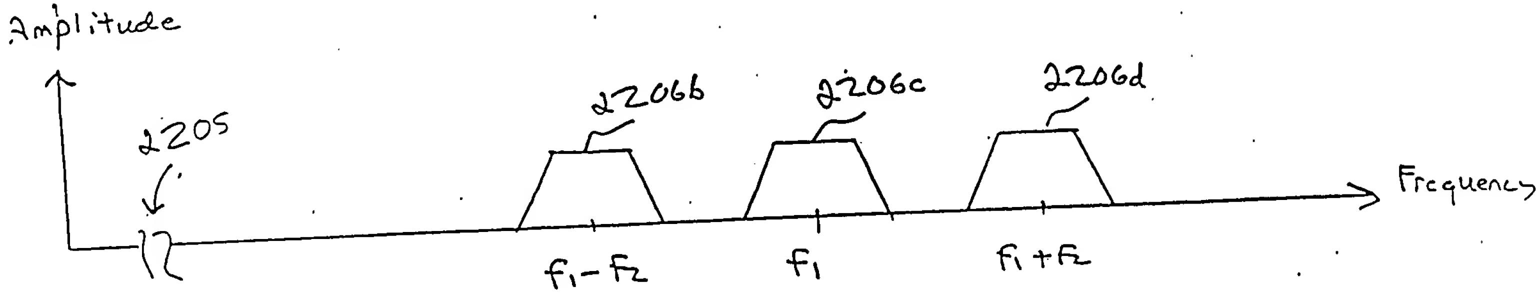


FIG. 22D

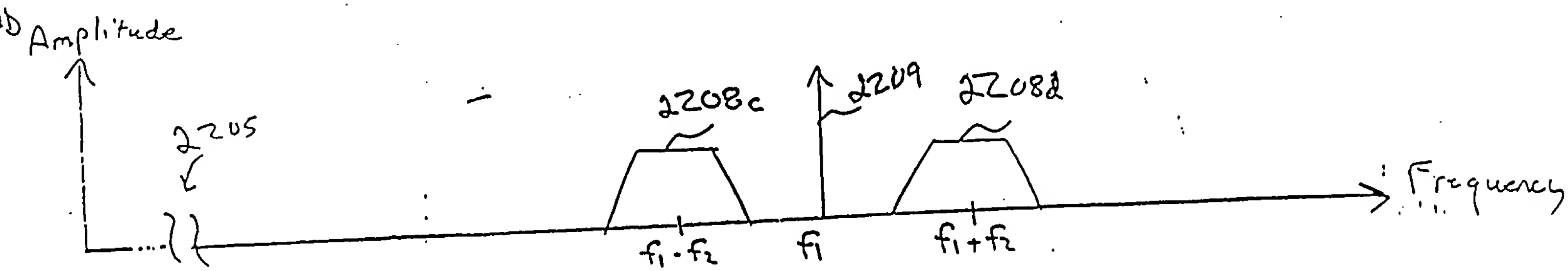


FIG. 22E

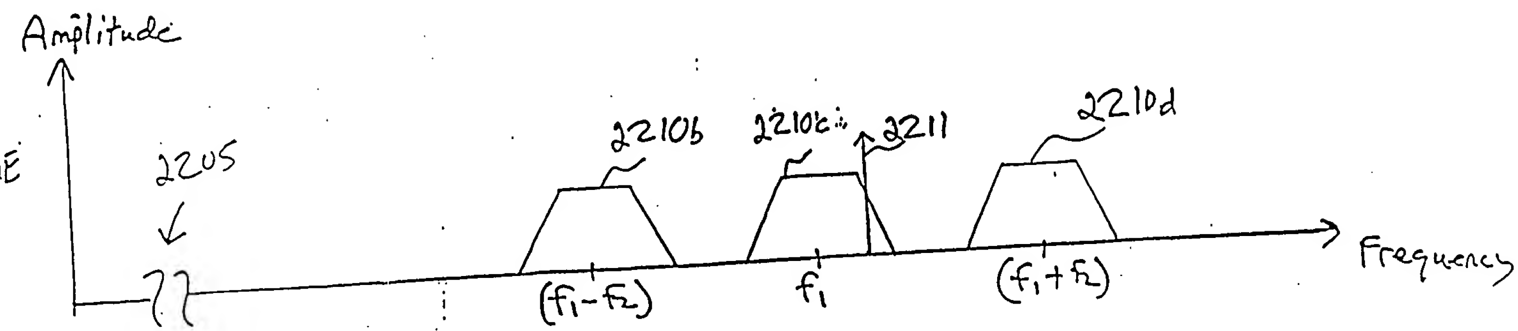
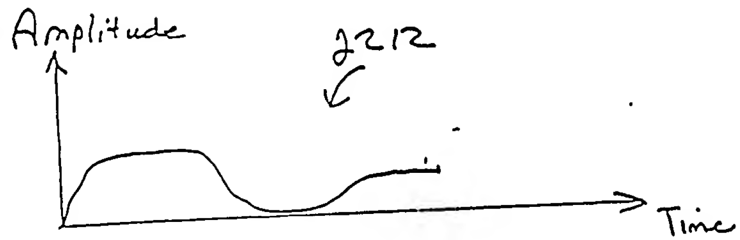
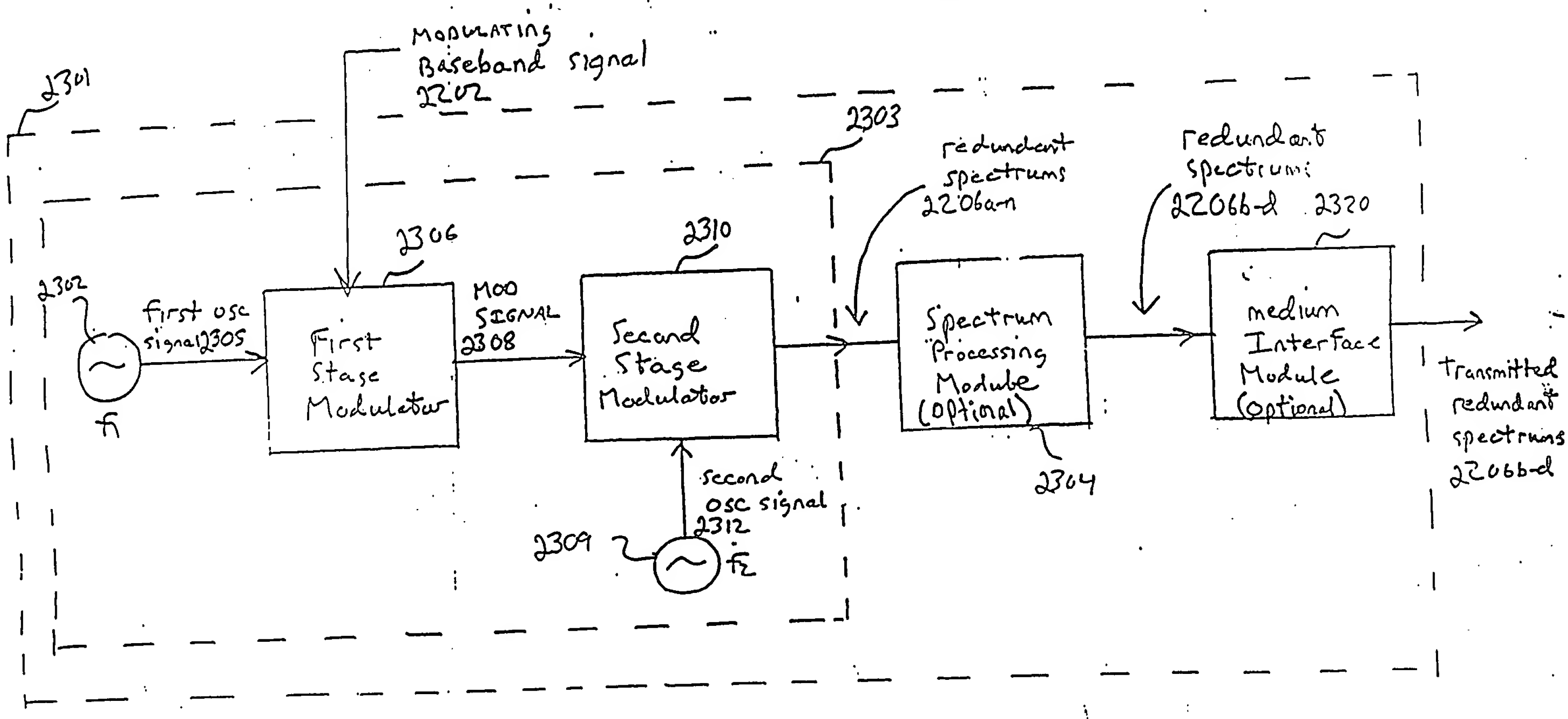


FIG. 22F





Modulating Baseband signal 2202
2301
2303
2302
first osc signal 2305
f1
2306
First Stage Modulator
MOD SIGNAL 2308
2310
Second Stage Modulator
second osc signal 2312
2309
f2
redundant spectrums 2206a-n
Spectrum Processing Module (Optional)
2304
redundant spectrums 2206b-d
2320
medium Interface Module (optional)
Transmitted redundant spectrums 2206b-d

FIG. 23A

FIG. 23B

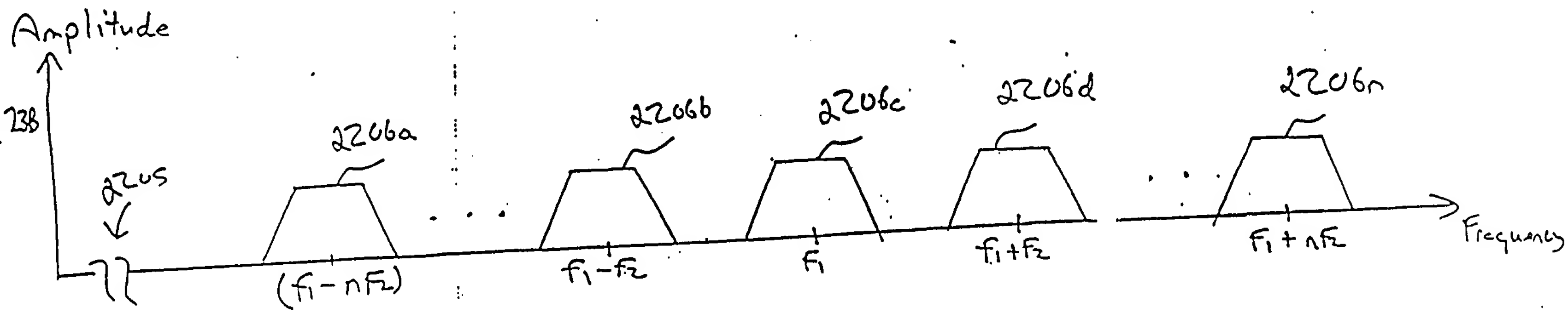
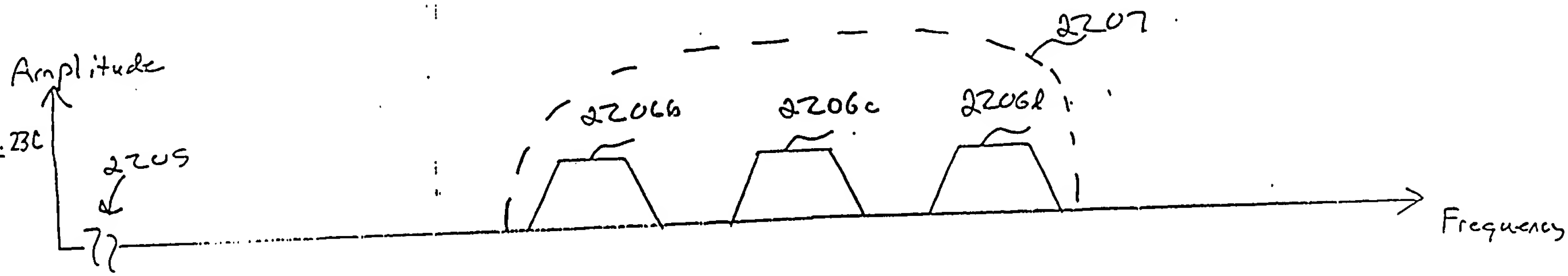


FIG. 23C



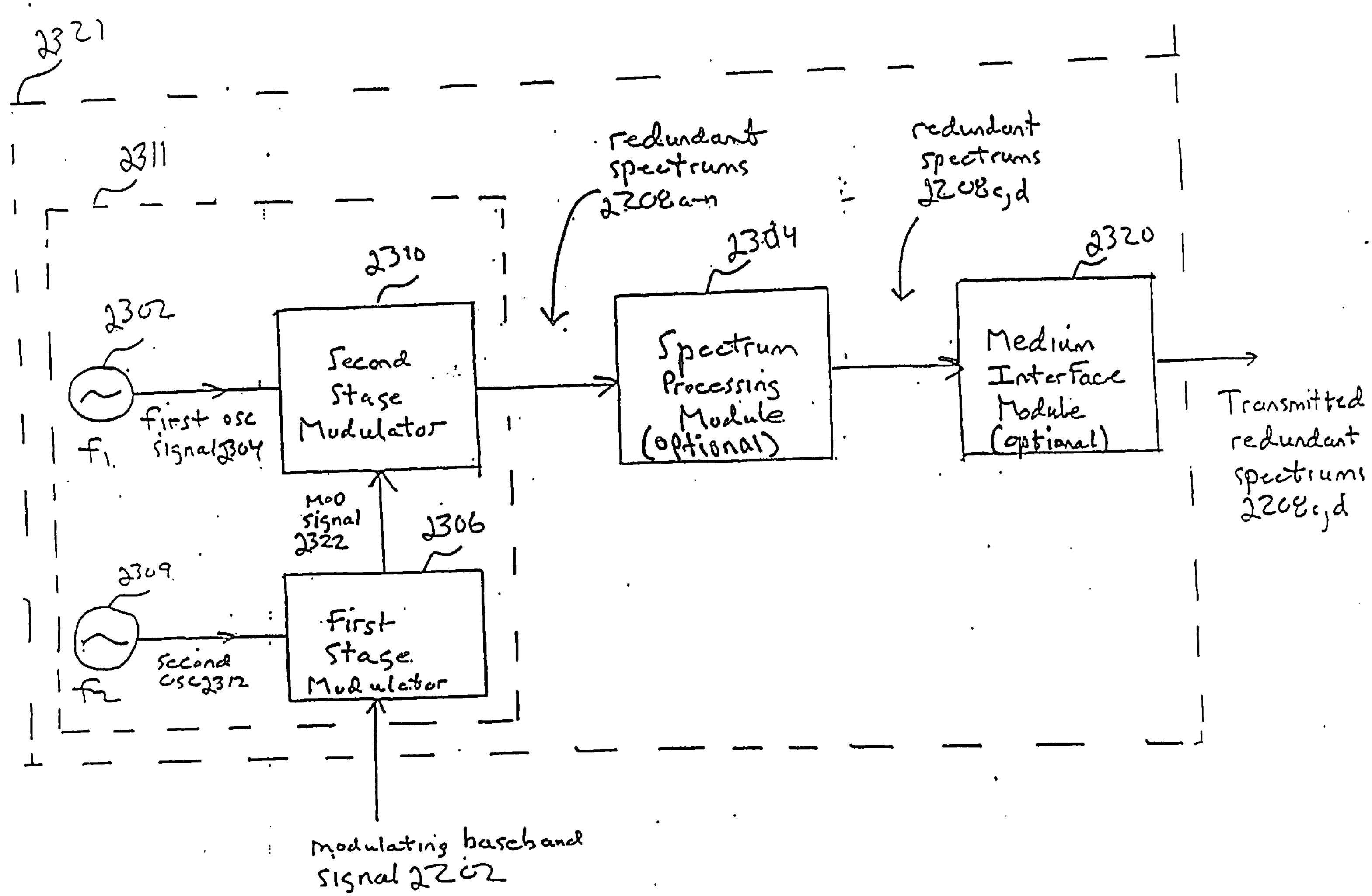

2321
2311
2302
f1
first osc signal 2304
2309
f2
second osc 2312
2310
Second Stage Modulator
MOO signal 2322
2306
First Stage Modulator
modulating baseband signal 2202
redundant spectrums 2208a-n
2304
Spectrum Processing Module (optional)
redundant spectrums 2208c,d
2320
Medium InterFace Module (optional)
Transmitted redundant spectrums 2208c,d

FIG. 23D

FIG. 23E

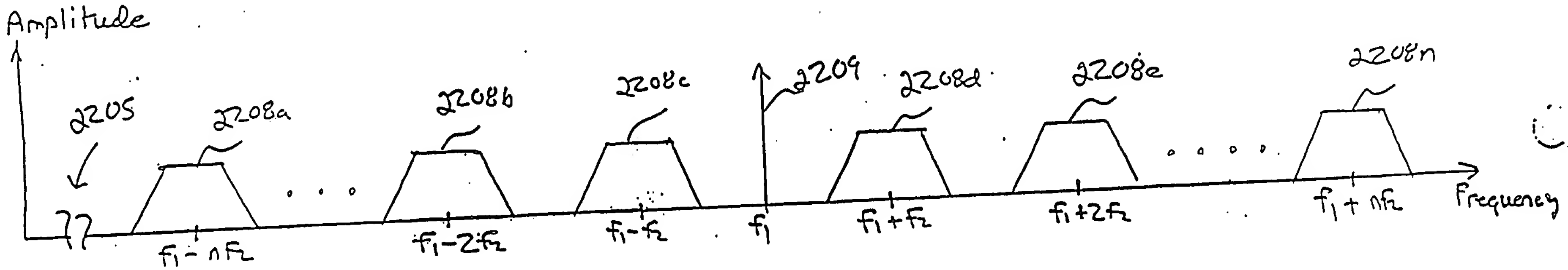
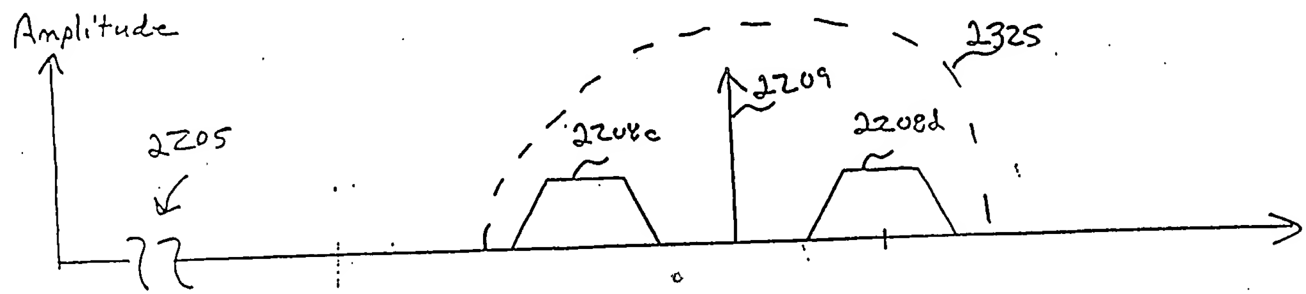


FIG. 23F



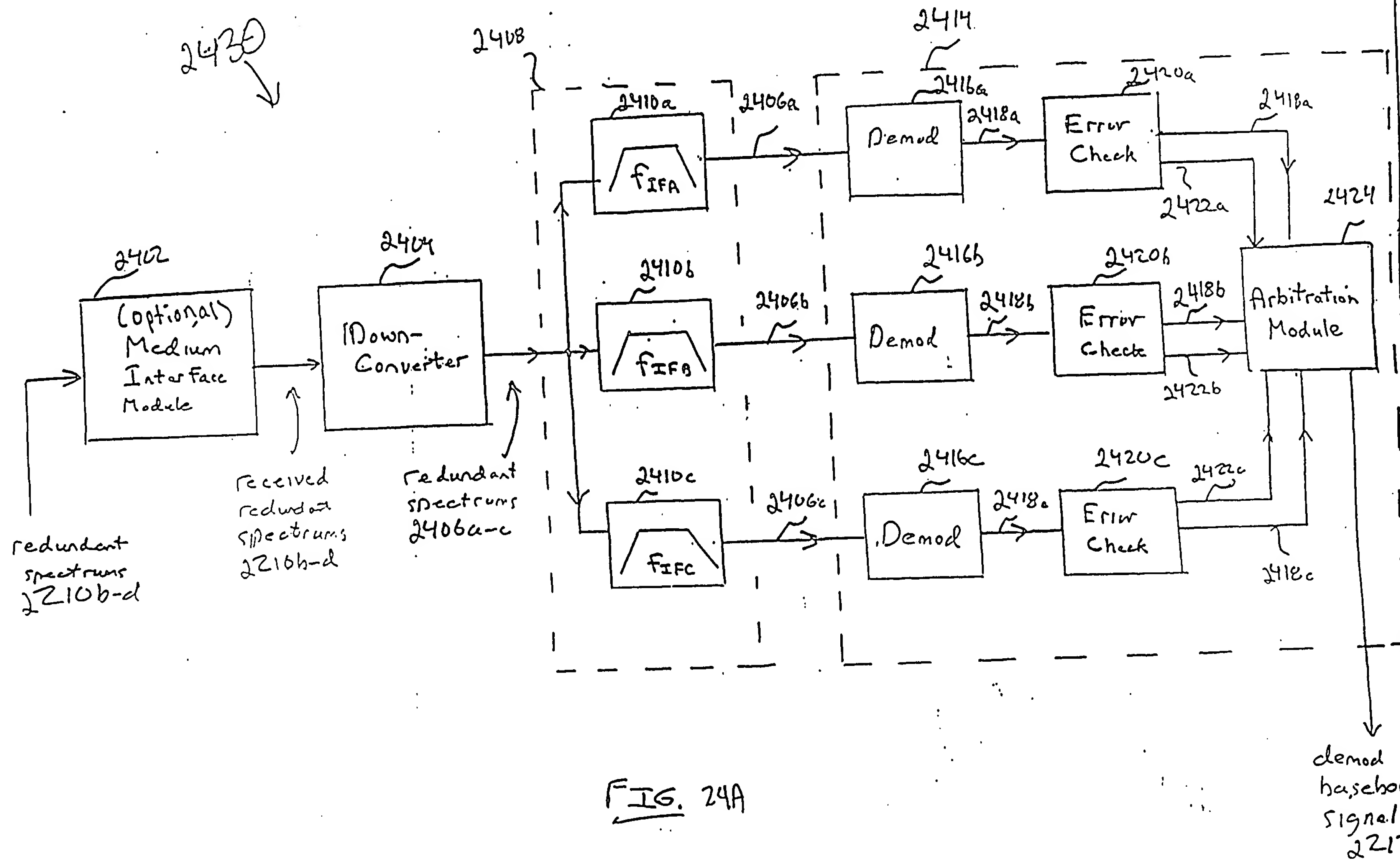

2430
2402
(optional) Medium Interface Module
2404
Down-Converter
redundant spectrums 2210b-d
received redundant spectrums 2216b-d
redundant spectrums 2406a-c
2408
2410a
f_{IFA}
2410b
f_{IFB}
2410c
f_{IFC}
2406a
2406b
2406c
2414
2416a
Demod
2416b
Demod
2416c
Demod
2418a
2418b
2418c
2420a
Error Check
2420b
Error Check
2420c
Error Check
2418a
2418b
2418c
2422a
2422b
2422c
2424
Arbitration Module
demod baseband signal 2212

FIG. 24A

00609055.060900

FIG. 24B

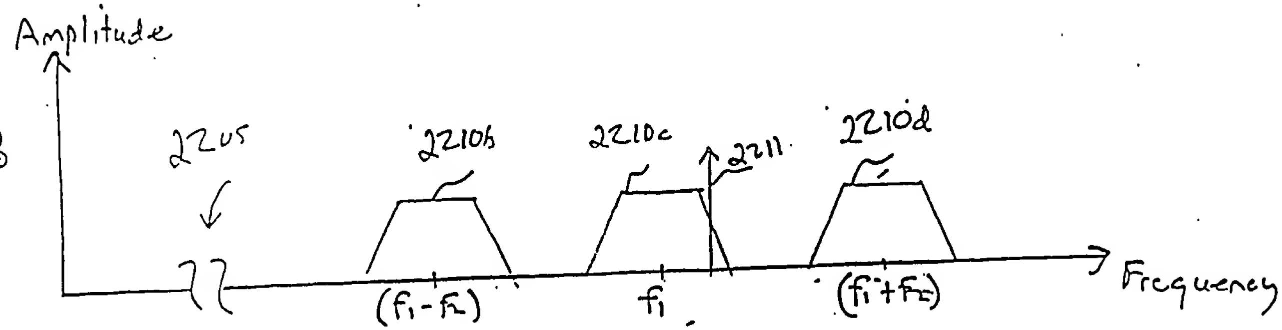


FIG. 24C.

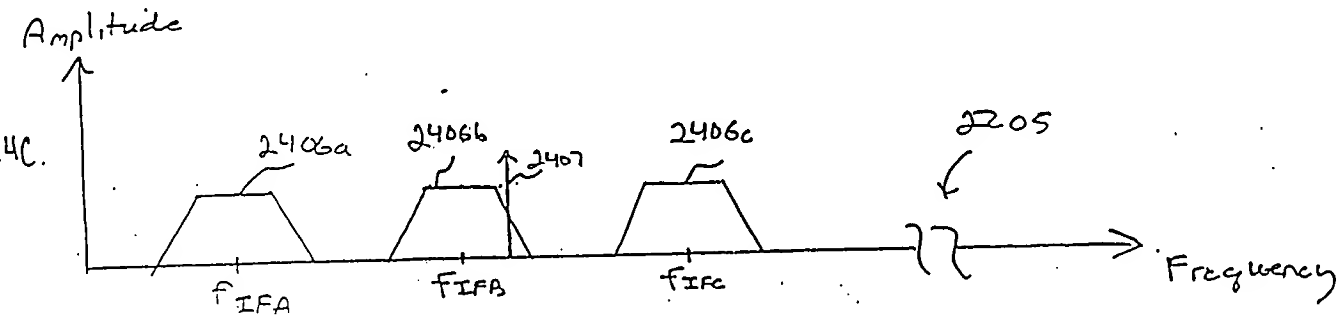


FIG. 24D

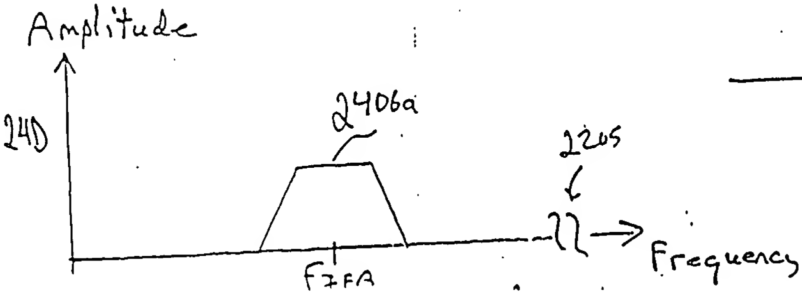


FIG. 24G

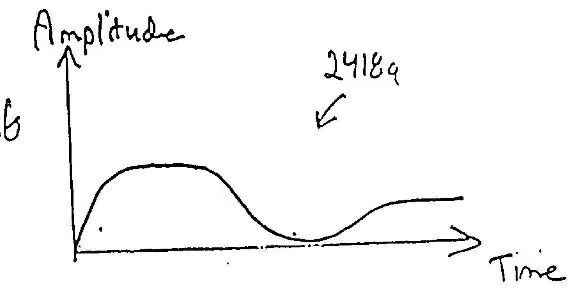


FIG. 24E

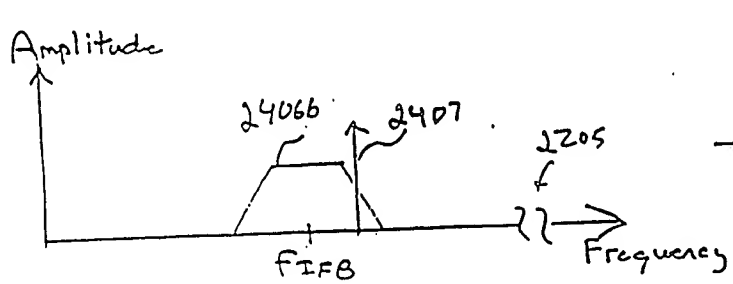


FIG. 24H

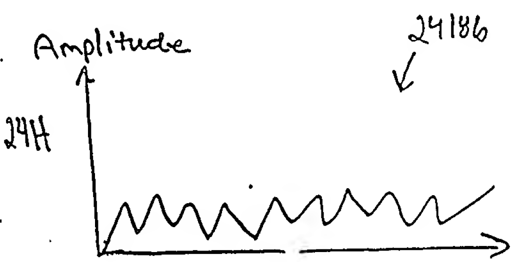


FIG 24F

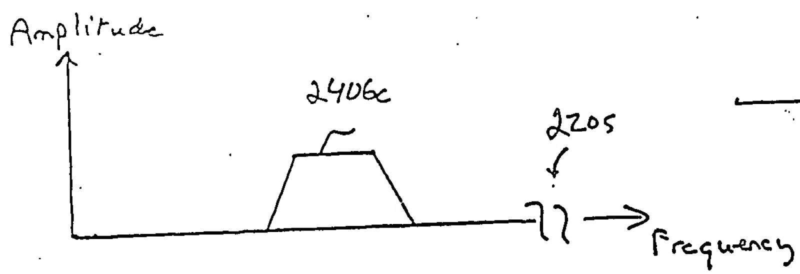
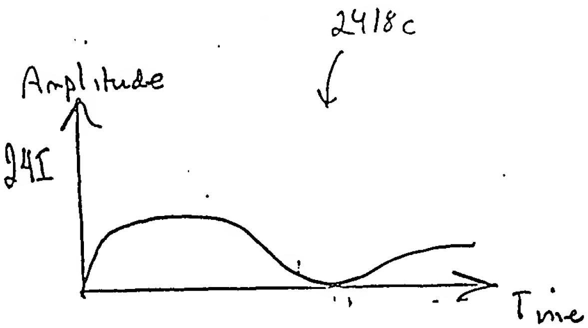


FIG. 24I



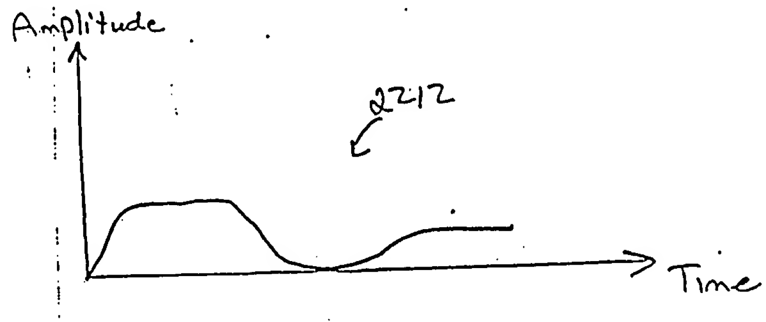


FIG. 24J

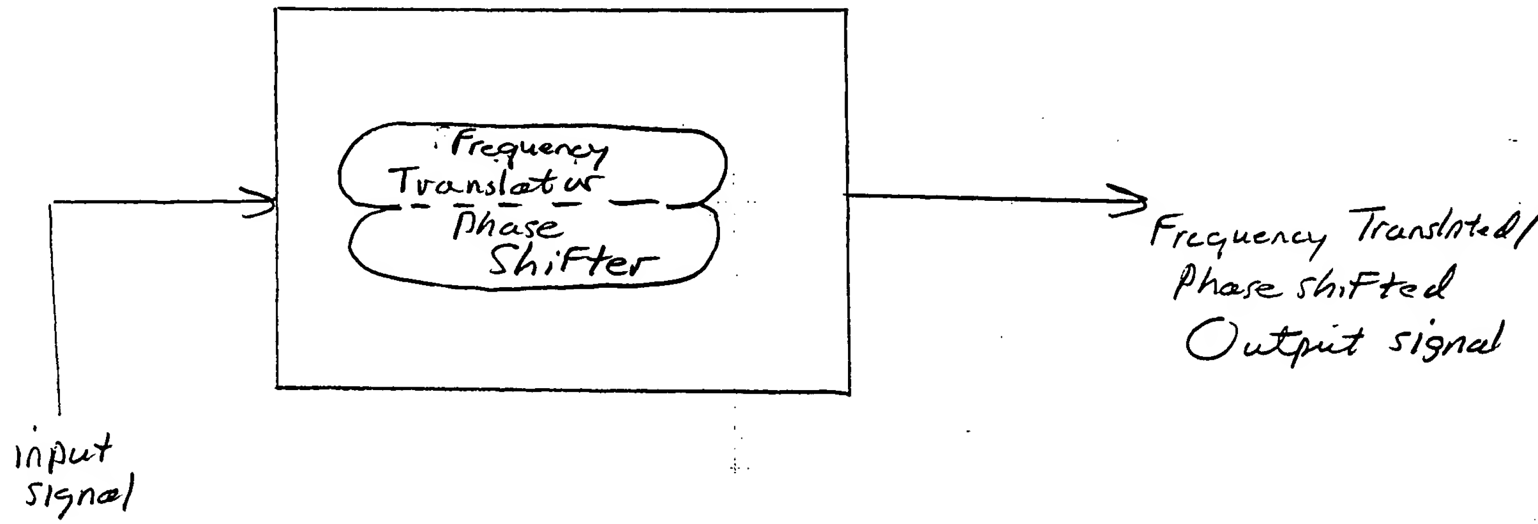

Frequency
Translator
Phase
Shifter
input
signal
Frequency Translated/
Phase shifted
Output signal

FIG. 25A

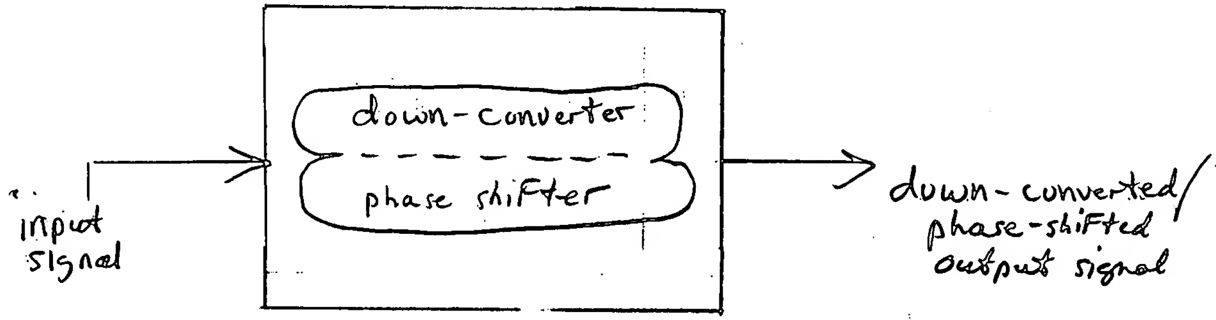


FIG. 25B

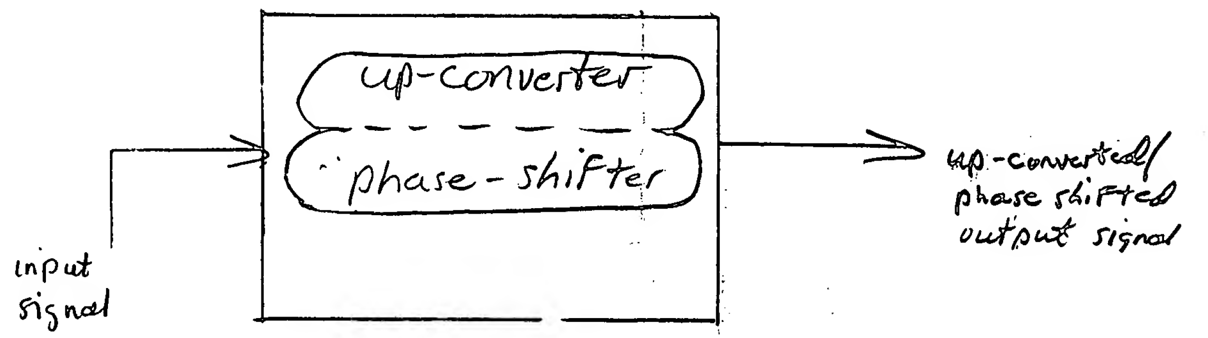


FIG. 25C

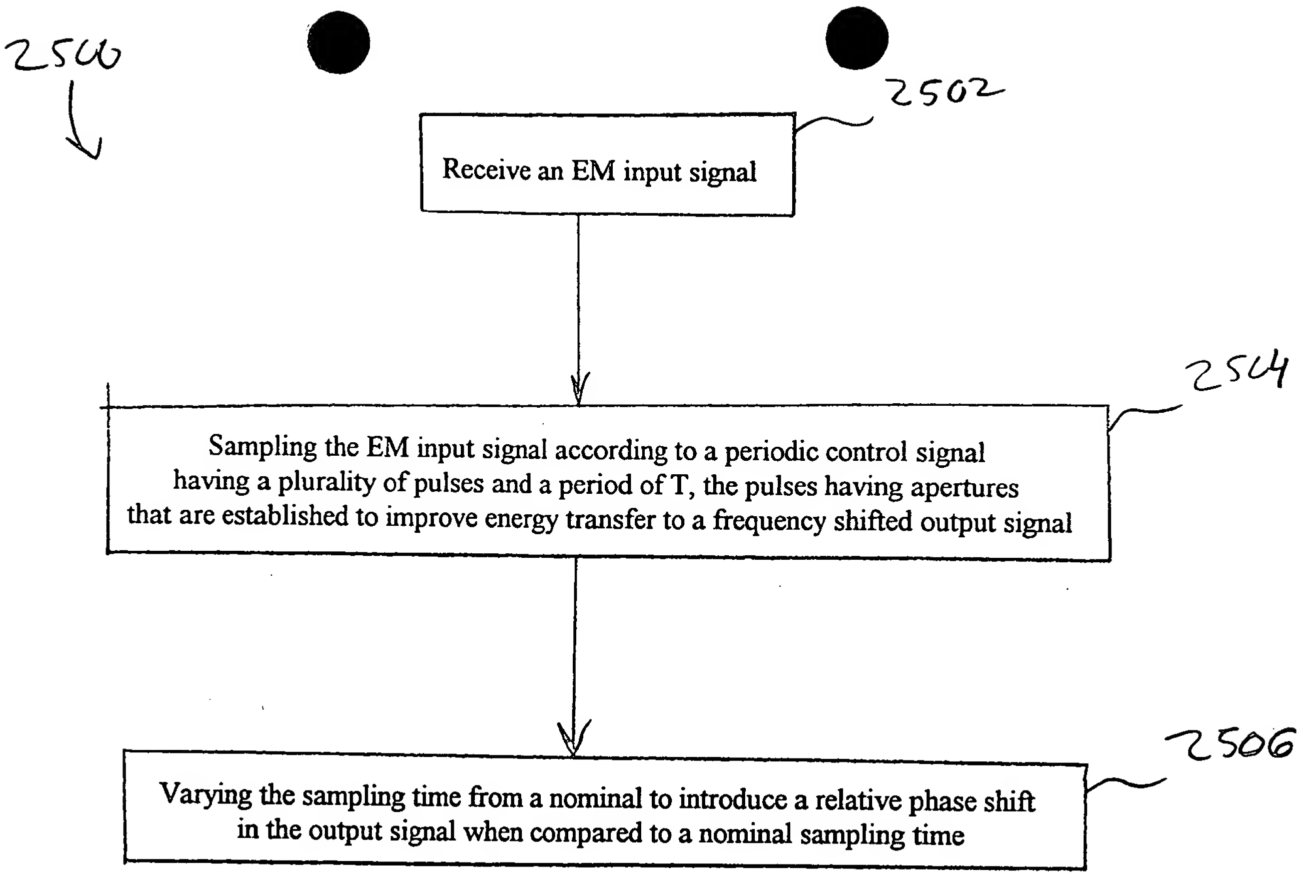

2500
2502
Receive an EM input signal
2504
Sampling the EM input signal according to a periodic control signal having a plurality of pulses and a period of T, the pulses having apertures that are established to improve energy transfer to a frequency shifted output signal
2506
Varying the sampling time from a nominal to introduce a relative phase shift in the output signal when compared to a nominal sampling time

FIG. 25D

FIG. 25E

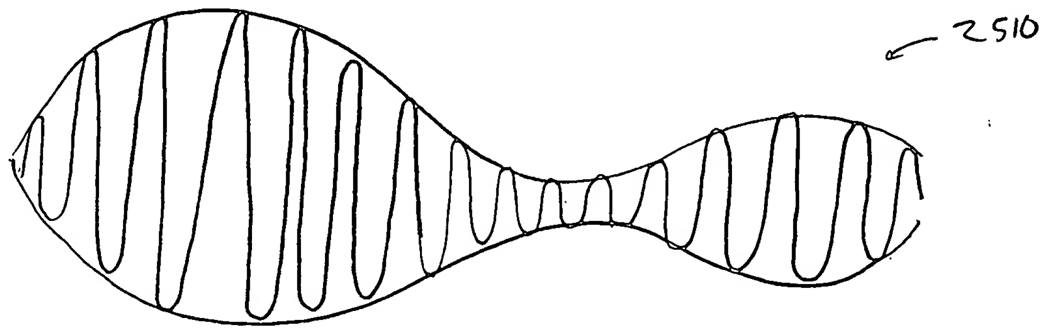


FIG. 25F

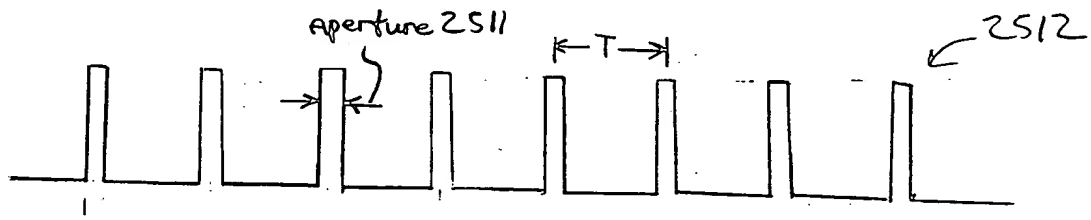


FIG. 25G

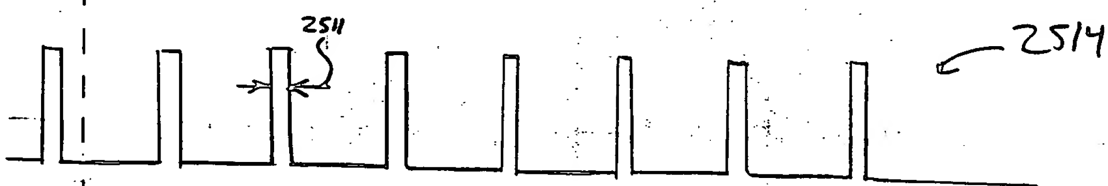
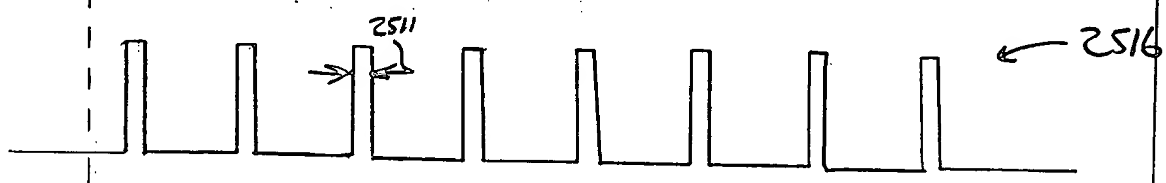


FIG. 25H



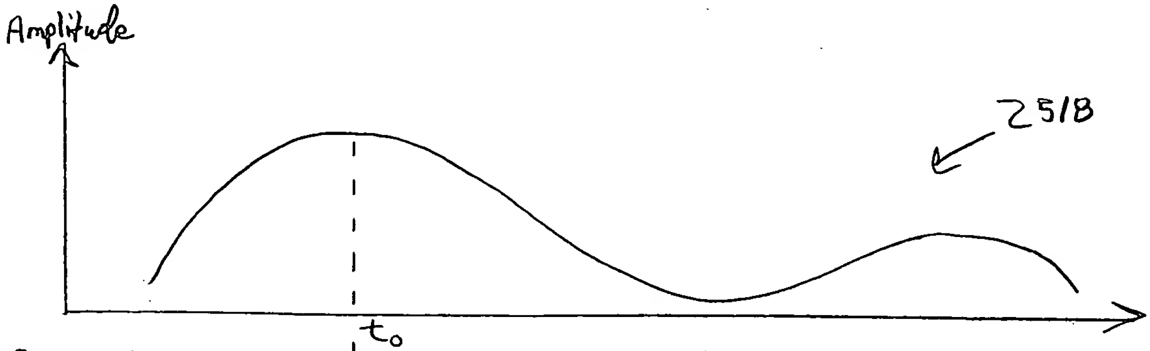


FIG. 25I

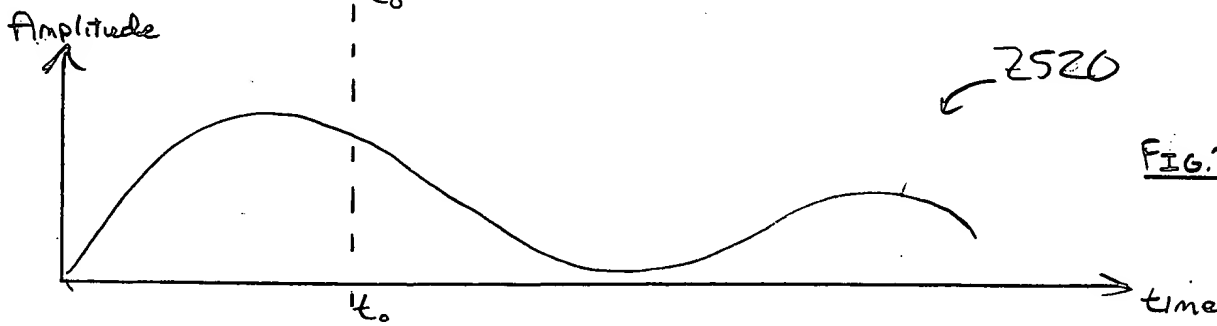


FIG. 25J

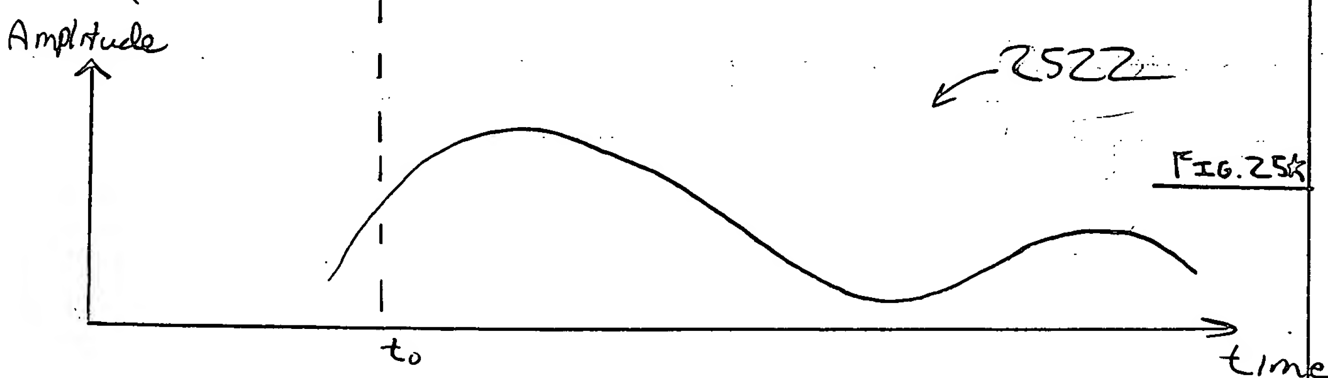


FIG. 25K

006090 " 55606560

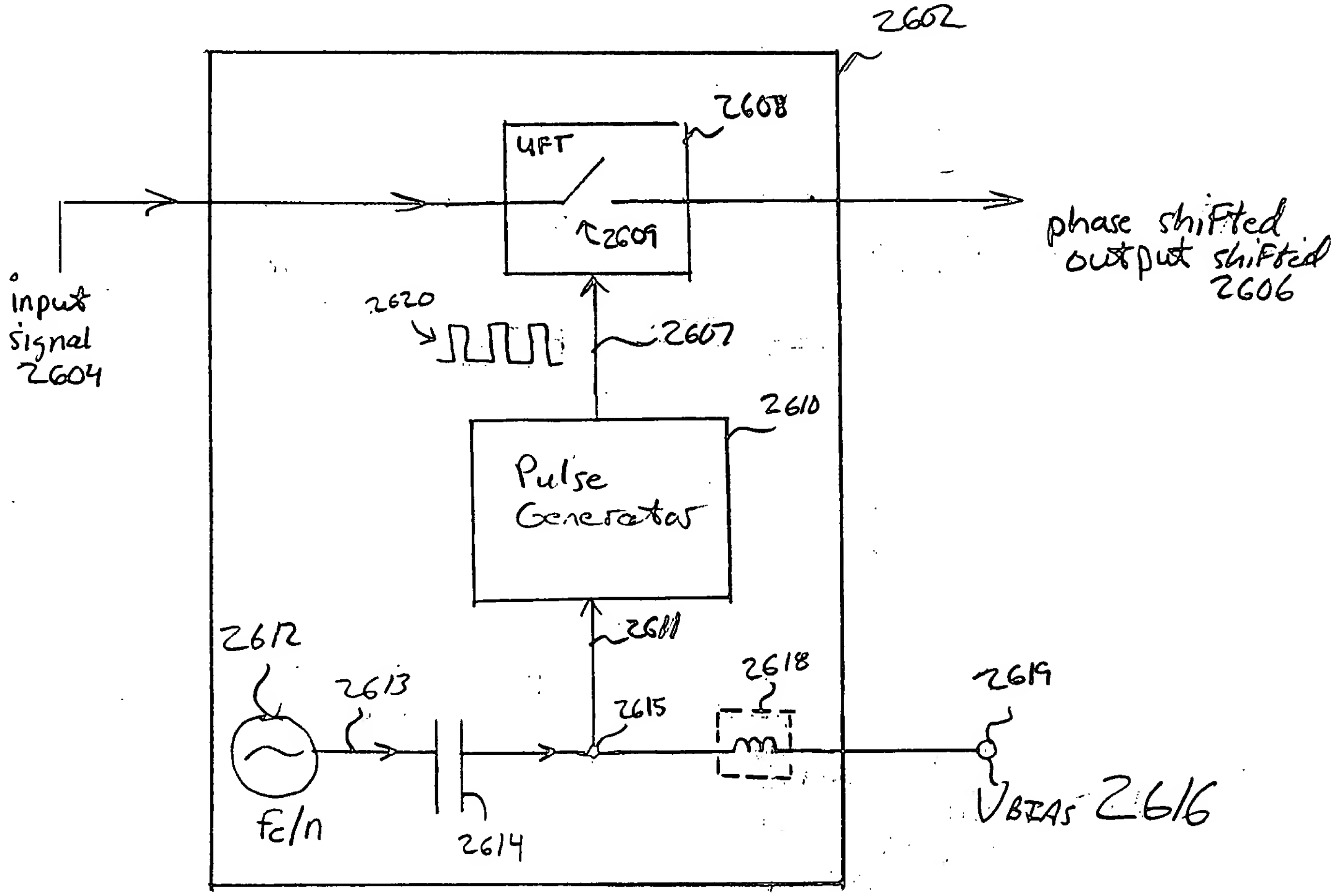


FIG. 26A

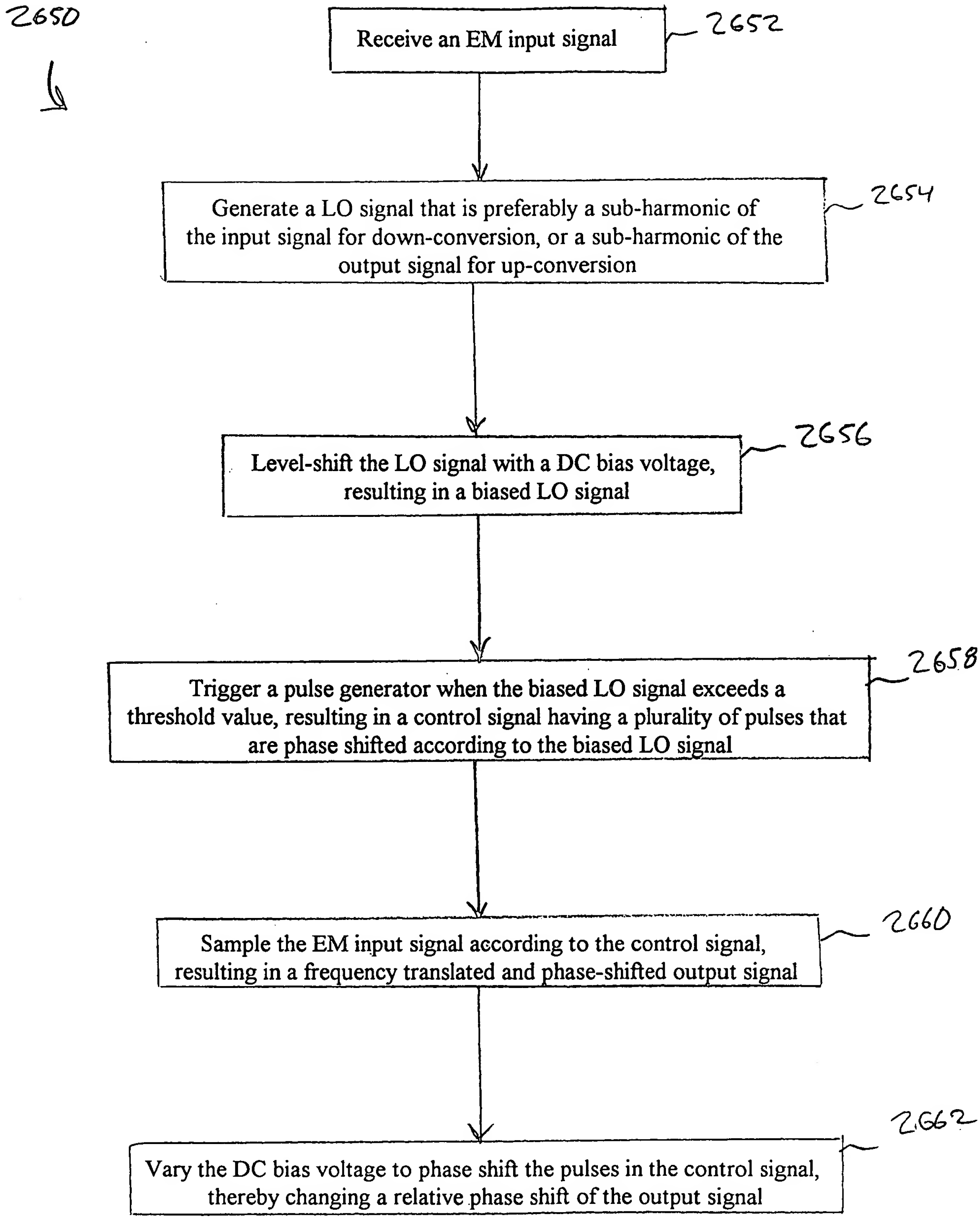

2650
Receive an EM input signal
2652
Generate a LO signal that is preferably a sub-harmonic of the input signal for down-conversion, or a sub-harmonic of the output signal for up-conversion
2654
Level-shift the LO signal with a DC bias voltage, resulting in a biased LO signal
2656
Trigger a pulse generator when the biased LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the biased LO signal
2658
Sample the EM input signal according to the control signal, resulting in a frequency translated and phase-shifted output signal
2660
Vary the DC bias voltage to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal
2662

FIG. 26B

FIG. 27A:
V_B = 0 volts

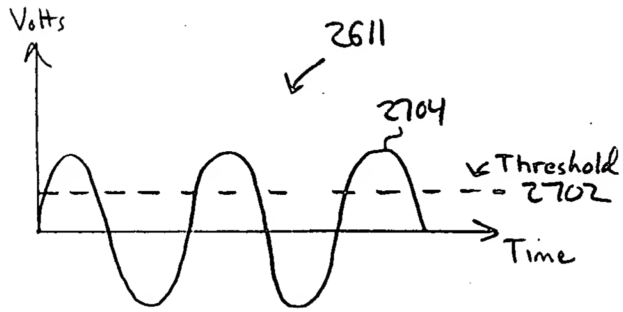


FIG. 27B:
V_B = +A volts

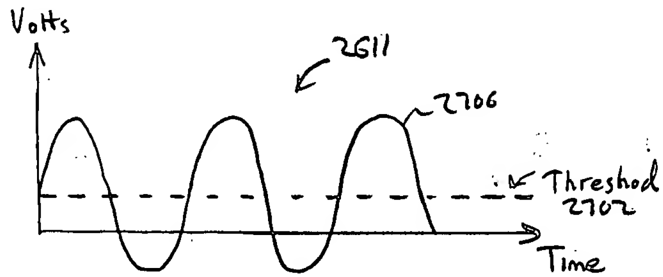


FIG. 27C:
V_B = -A volts

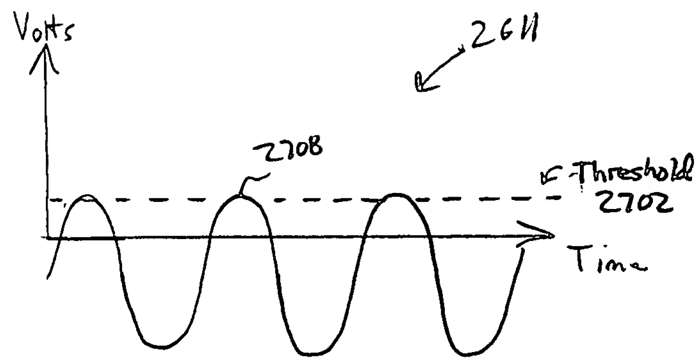
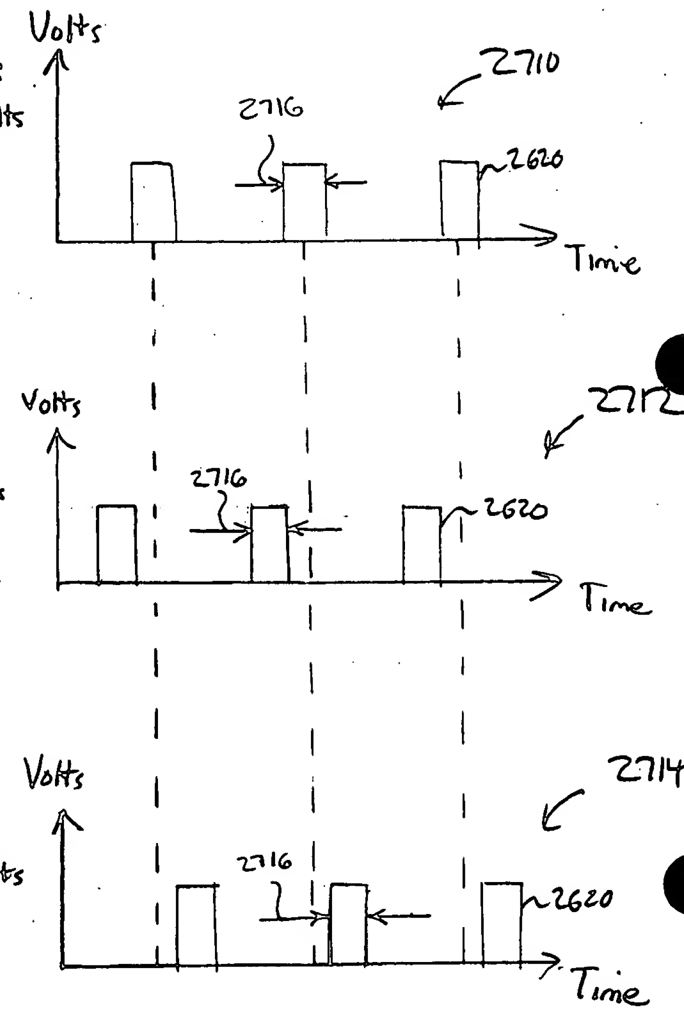


FIG. 27D:
V_B = 0 volts

FIG. 27E:
V_B = +A volts

FIG. 27F:
V_B = -A volts



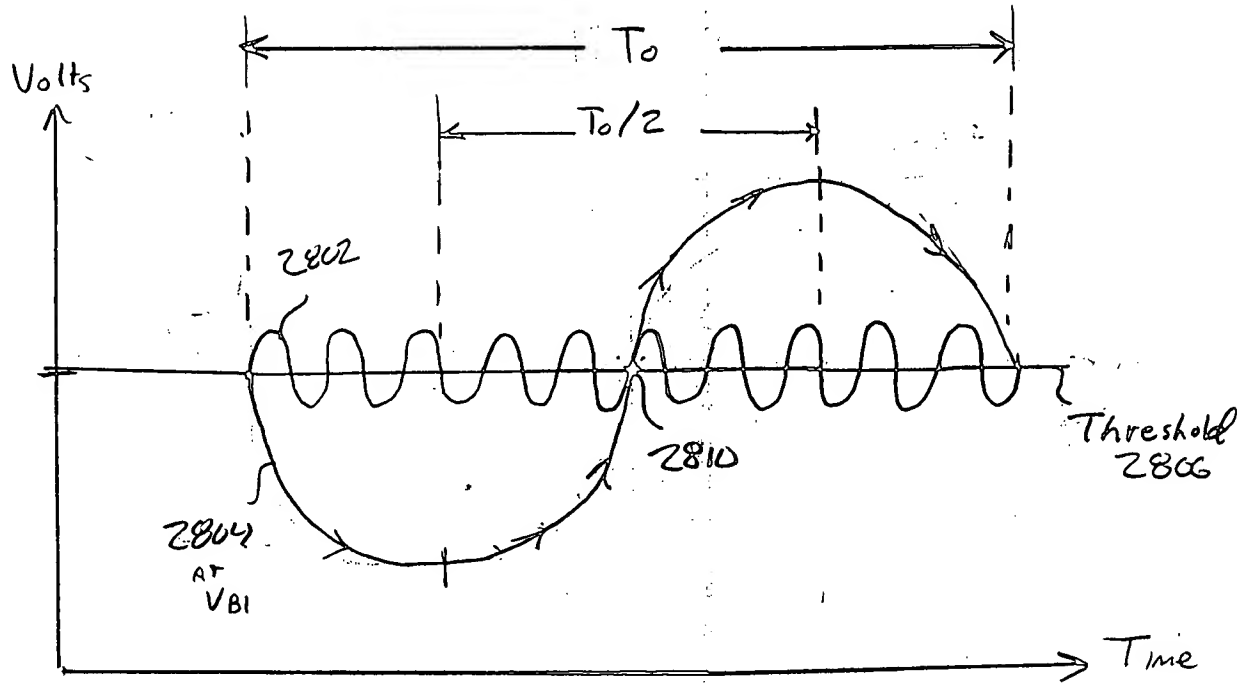


FIG. 28A

09909555.060900

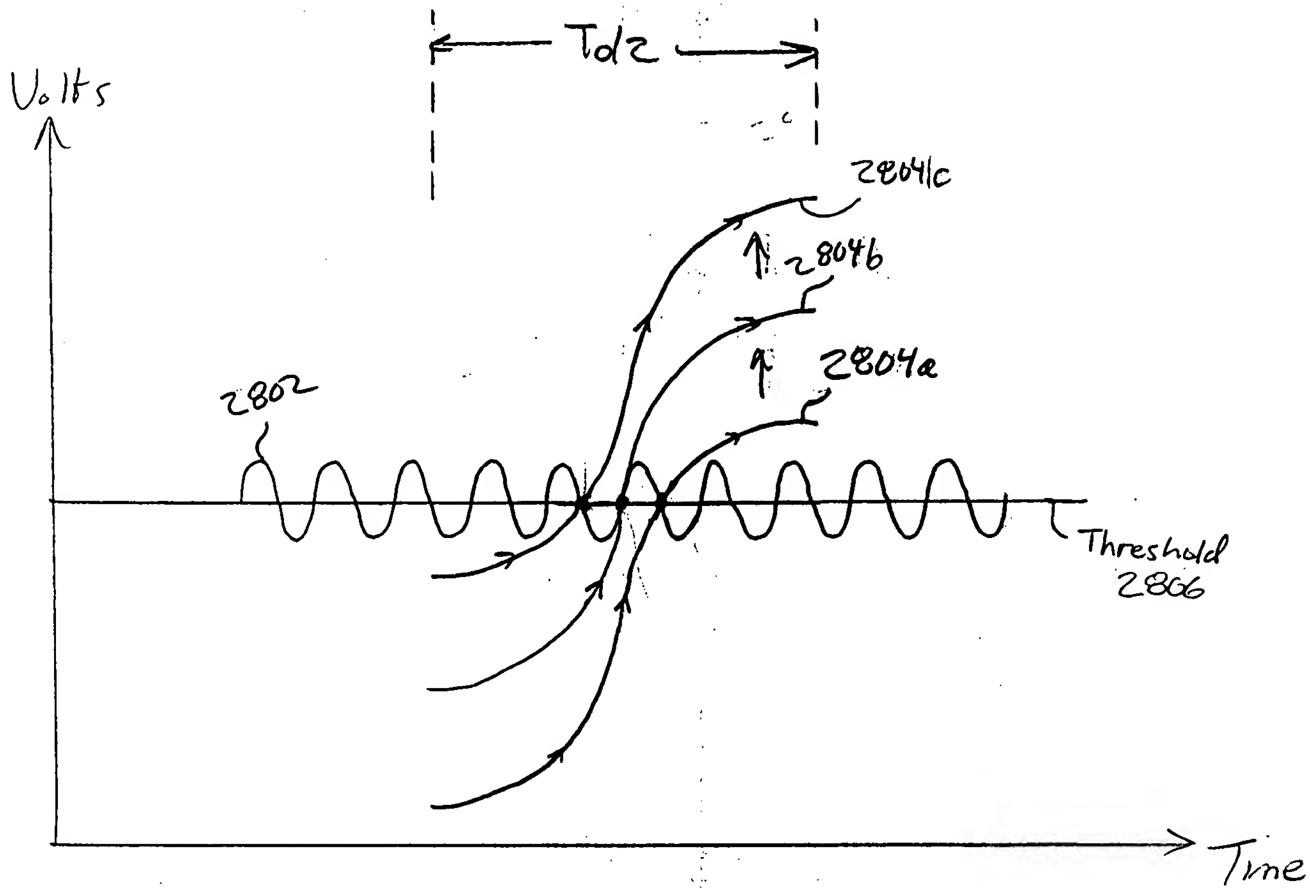


FIG. 28B

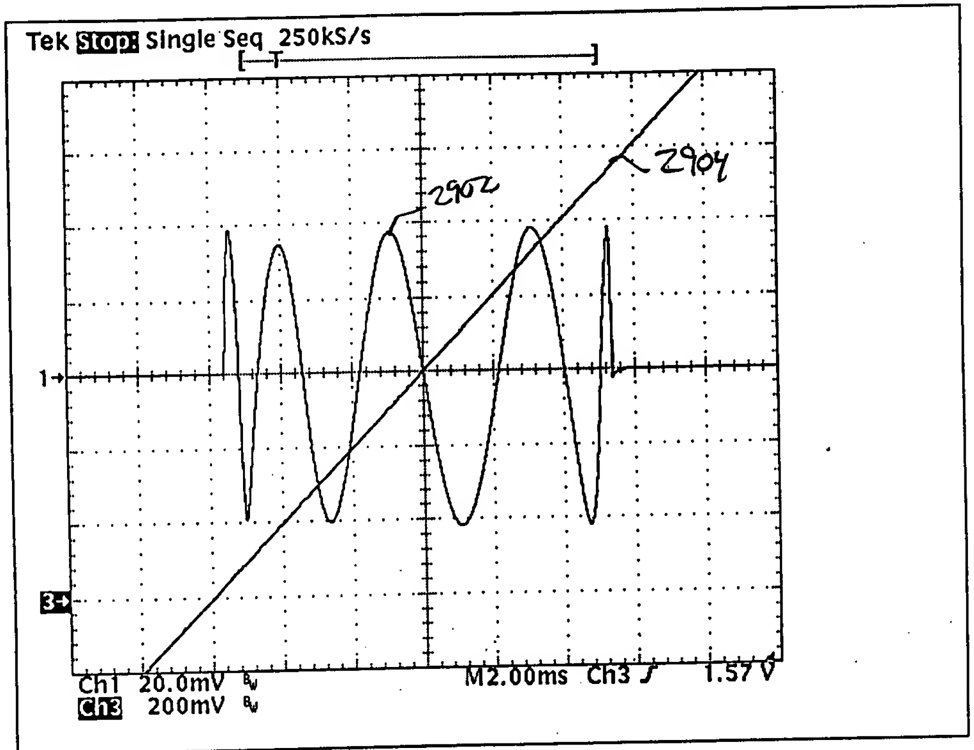
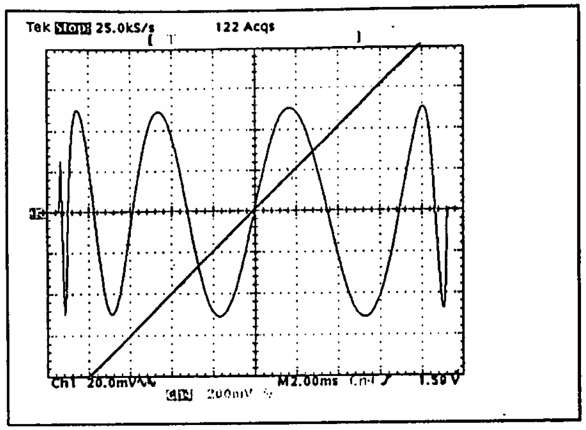

Tek Stop: Single Seq 250kS/s
2902
2904
1→
3→
Ch1 20.0mV
Ch3 200mV
M2.00ms Ch3 ƒ 1.57 V

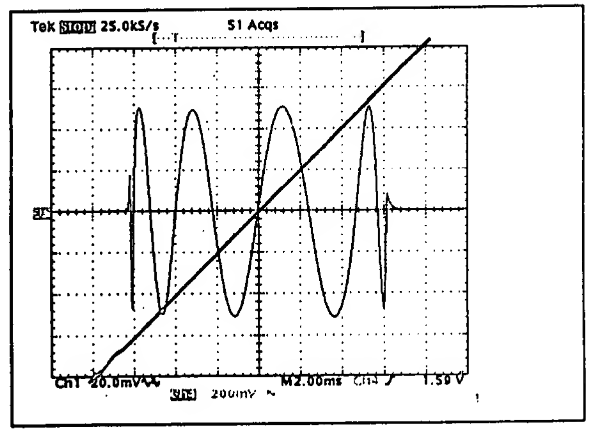
FIG. 29

FIG. 30A

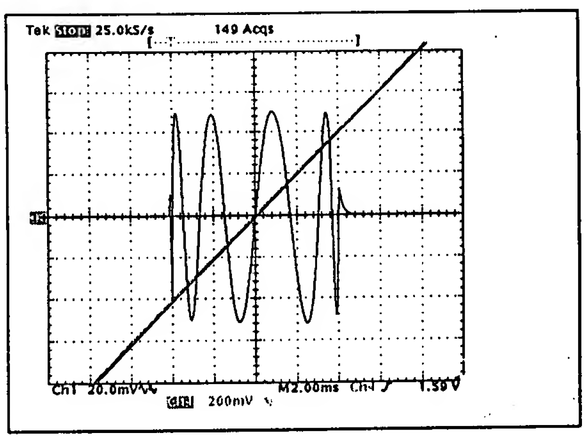


LO amplitude=1.415 $V_{p\text{-}p}$.

FIG. 30B

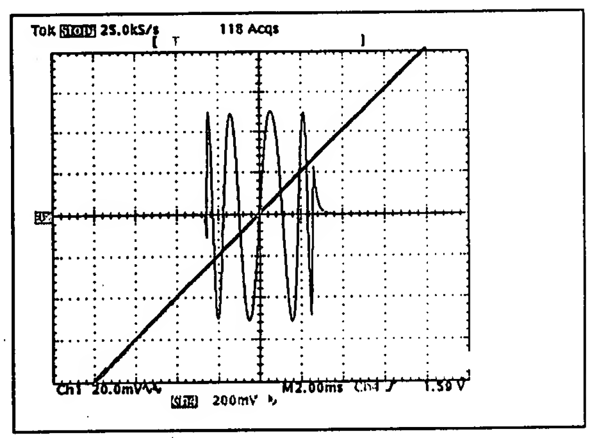


LO amplitude=1.002 $V_{p\text{-}p}$.



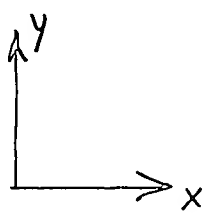
LO amplitude=0.710 $V_{p\text{-}p}$.

FIG. 30C



LO amplitude=0.502 $V_{p\text{-}p}$.

FIG. 30D



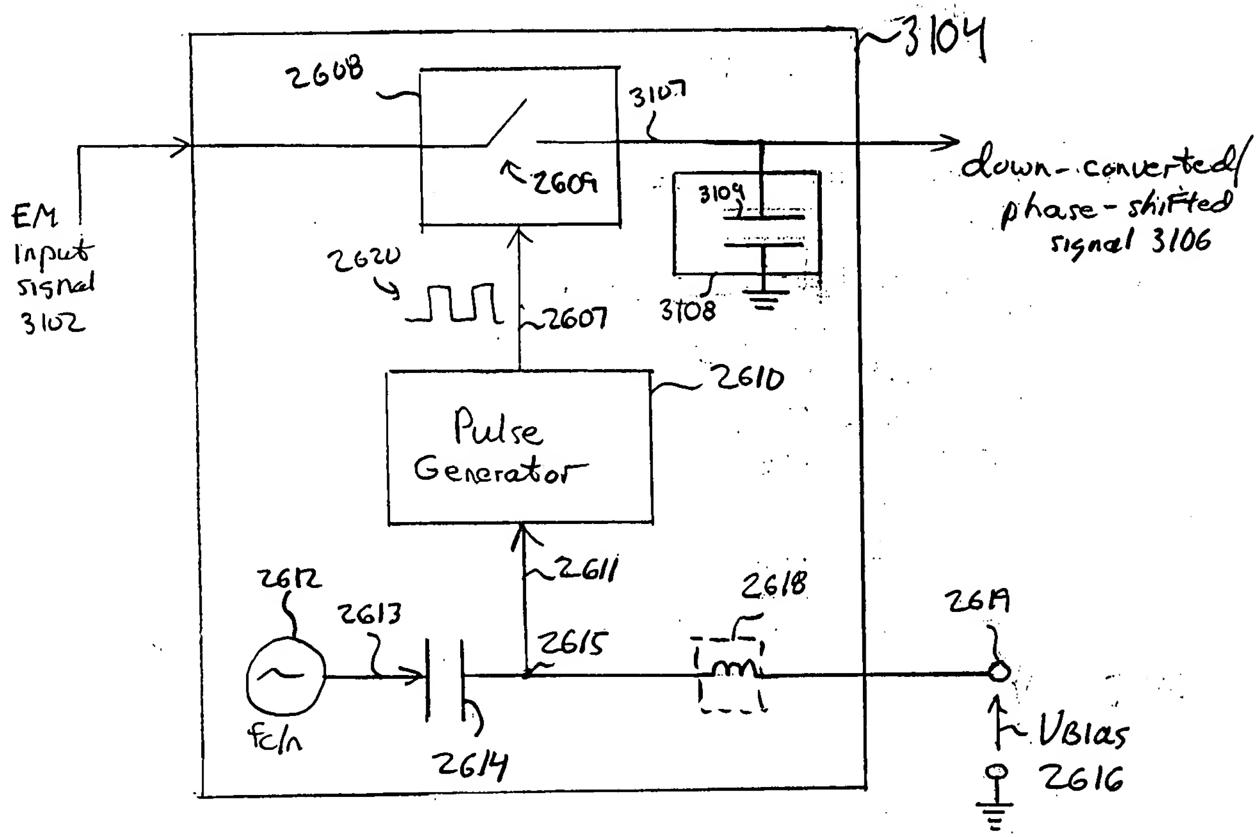

3104
2608
3107
2609
EM input signal 3102
3109
3108
down-converted/ phase-shifted signal 3106
2620
2607
2610
Pulse Generator
2611
2612
2613
2615
2618
2617
fc/n
2614
VBIAS 2616

FIG. 31A

3150

Receive an EM input signal 3152

Generate a LO signal that is preferably a sub-harmonic of the input signal for down-conversion to baseband, or offset from a sub-harmonic of the input signal for down-conversion to an IF frequency 3154

Level-shift the LO signal with a DC bias voltage, resulting in a biased LO signal 3156

Trigger a pulse generator when the biased LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the biased LO signal, wherein the pulses of the control signal are a non-negligible fraction of a period of the EM input signal to be down-converted 3158

Sample the EM input signal according to the periodic control signal to transfer non-negligible amounts of energy to the resulting undersamples 3160

Store and integrate the successive undersamples, resulting in a down-converted output signal 3162

Vary the DC bias voltage to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal 3164

FIG. 31B

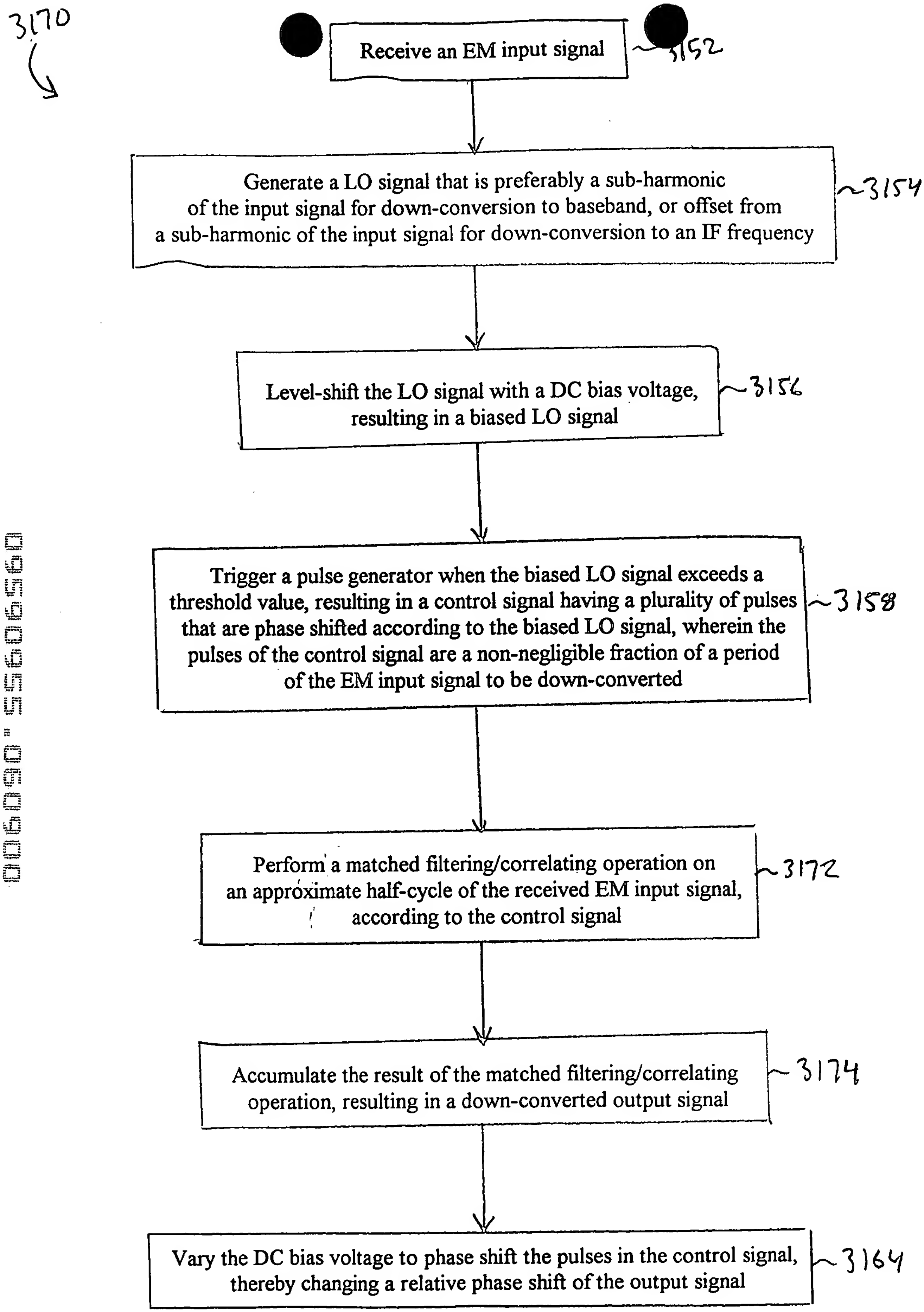

3170
Receive an EM input signal
3152
Generate a LO signal that is preferably a sub-harmonic of the input signal for down-conversion to baseband, or offset from a sub-harmonic of the input signal for down-conversion to an IF frequency
3154
Level-shift the LO signal with a DC bias voltage, resulting in a biased LO signal
3156
Trigger a pulse generator when the biased LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the biased LO signal, wherein the pulses of the control signal are a non-negligible fraction of a period of the EM input signal to be down-converted
3158
Perform a matched filtering/correlating operation on an approximate half-cycle of the received EM input signal, according to the control signal
3172
Accumulate the result of the matched filtering/correlating operation, resulting in a down-converted output signal
3174
Vary the DC bias voltage to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal
3164

FIG 31C

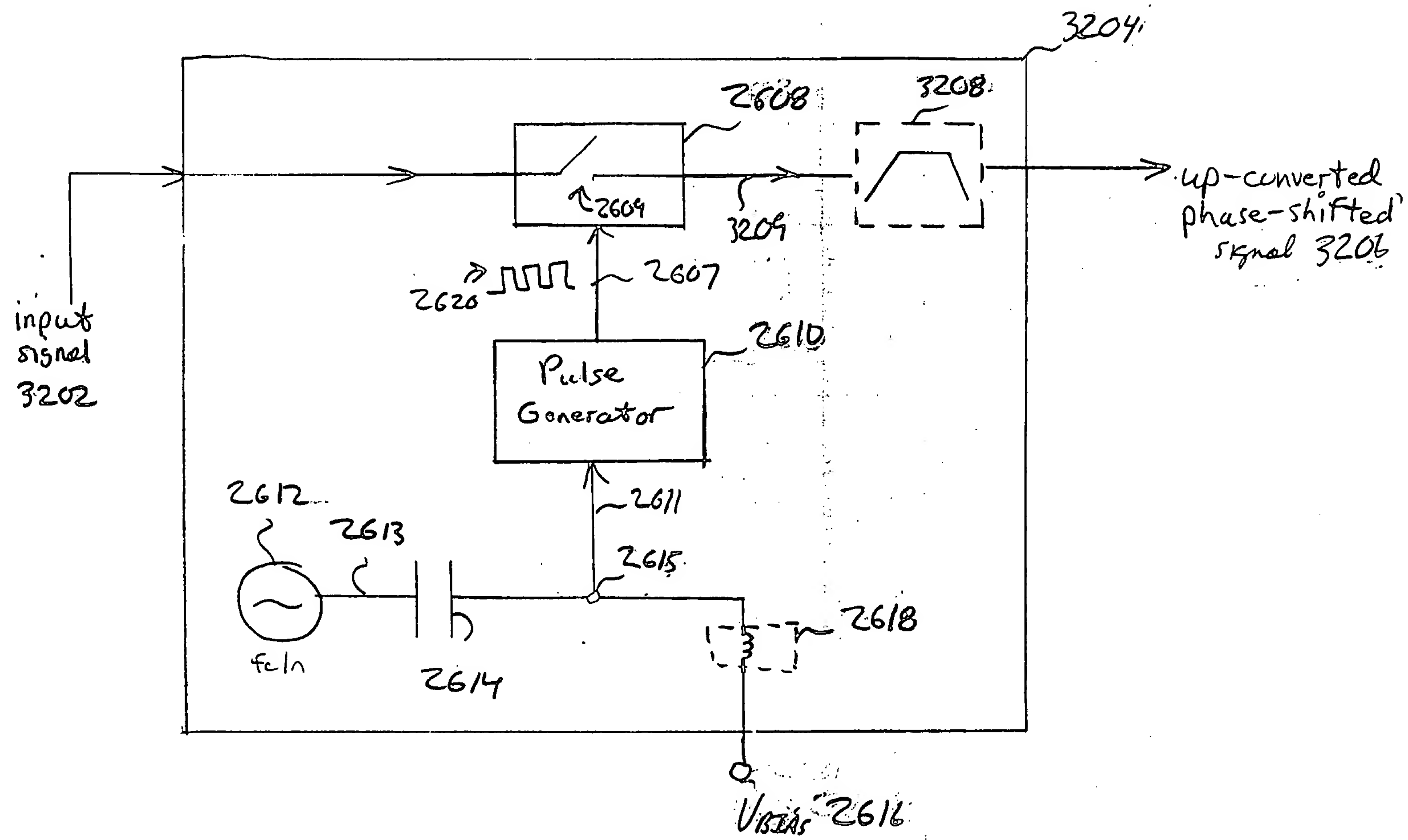

3204
2608
3208
up-converted
phase-shifted
signal 3206
input
signal
3202
2609
3209
2620
2607
2610
Pulse
Generator
2612
2613
2611
2615
2618
fclk
2614
VBIAS 2616

FIG. 32A

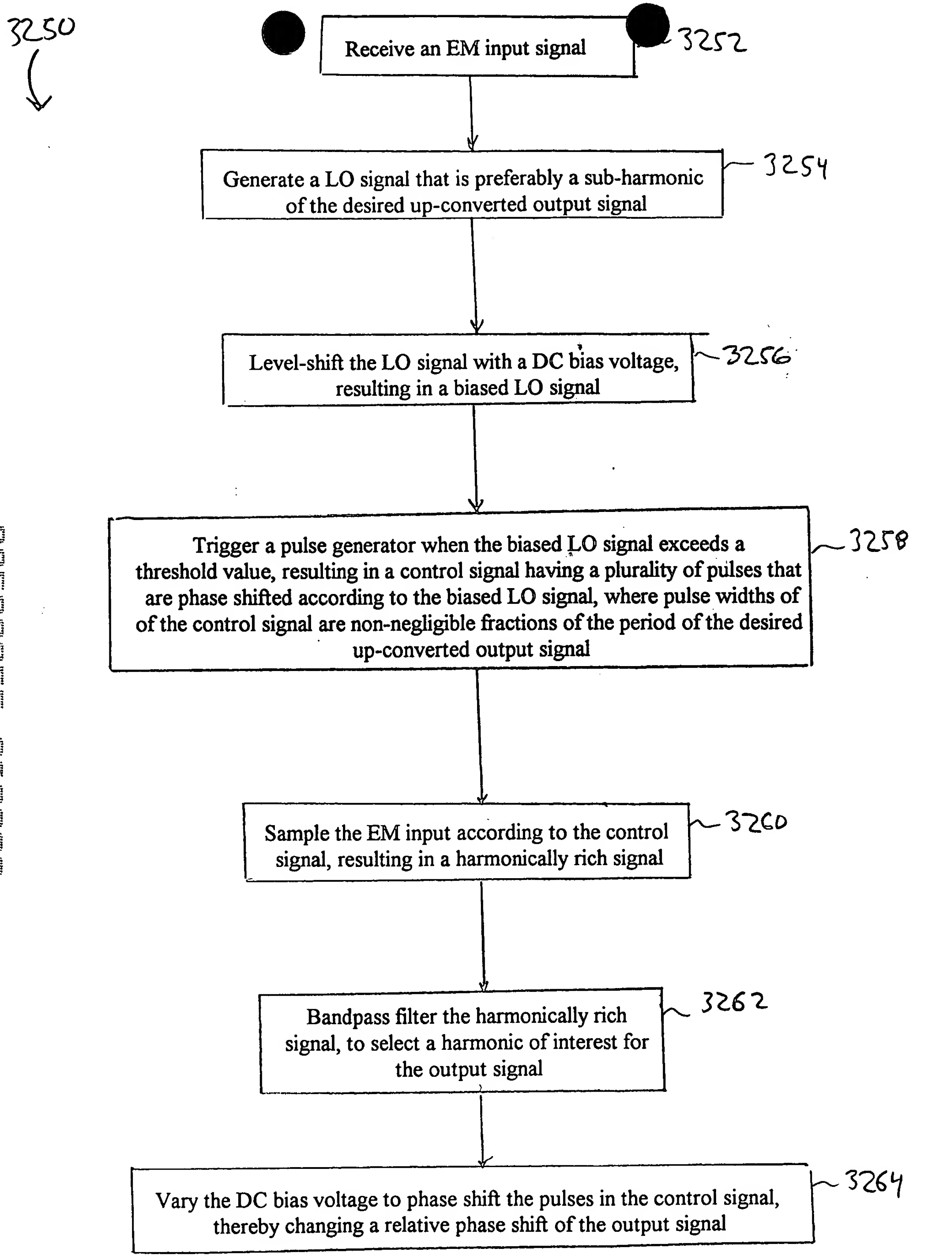

3250
Receive an EM input signal
3252
Generate a LO signal that is preferably a sub-harmonic of the desired up-converted output signal
3254
Level-shift the LO signal with a DC bias voltage, resulting in a biased LO signal
3256
Trigger a pulse generator when the biased LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the biased LO signal, where pulse widths of of the control signal are non-negligible fractions of the period of the desired up-converted output signal
3258
Sample the EM input according to the control signal, resulting in a harmonically rich signal
3260
Bandpass filter the harmonically rich signal, to select a harmonic of interest for the output signal
3262
Vary the DC bias voltage to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal
3264

FIG. 32B

006090"55606560

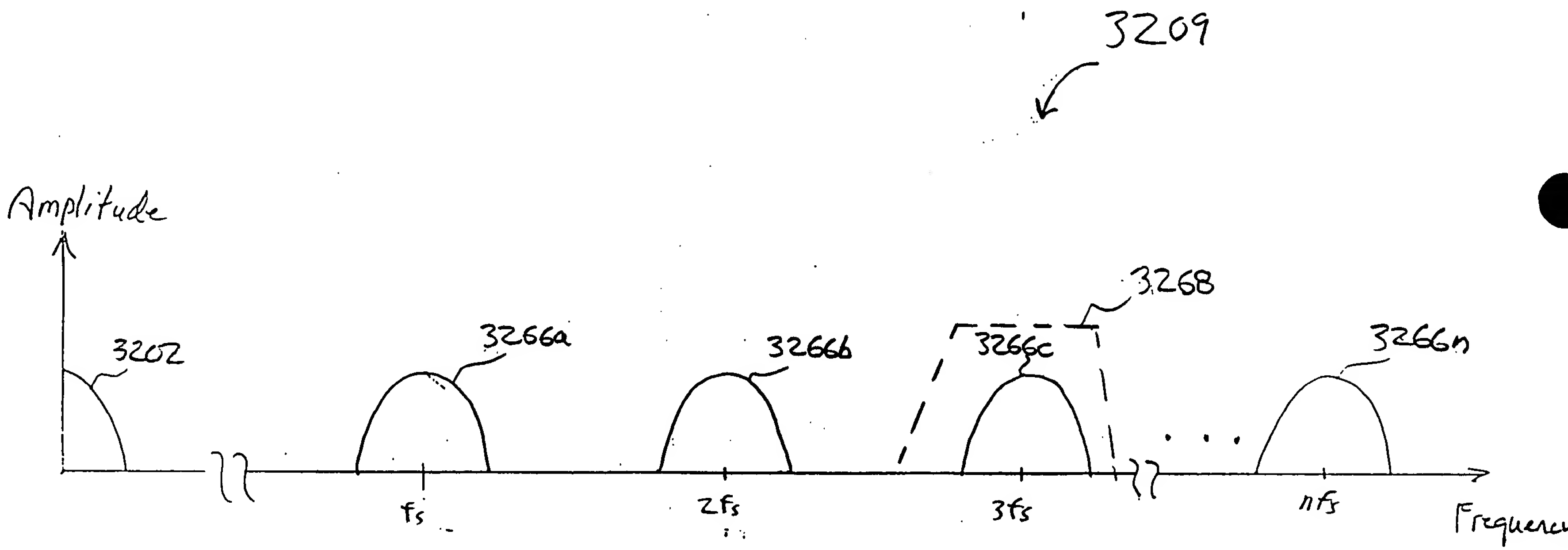
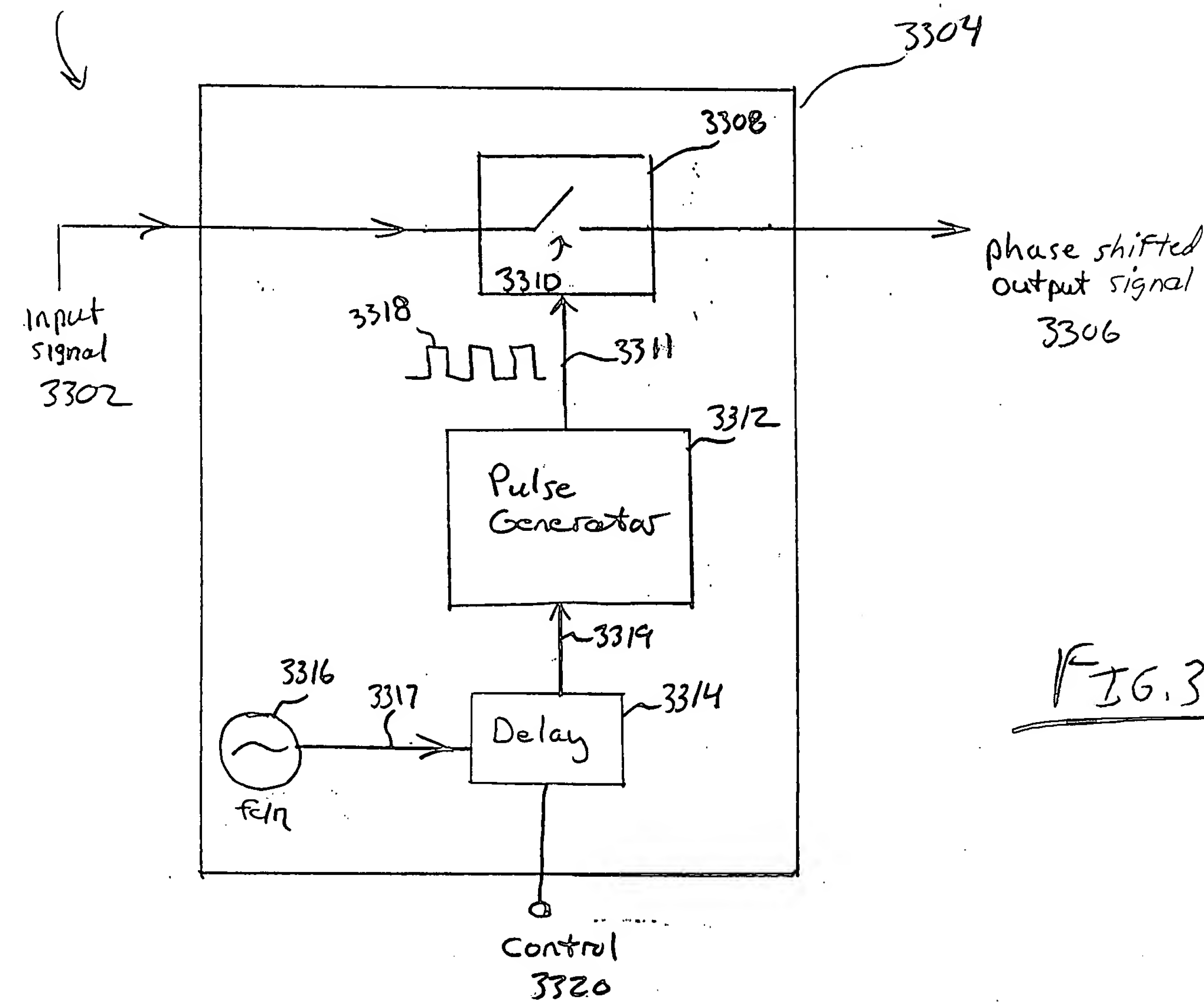


FIG. 32C



3304
3308
3310
input signal 3302
phase shifted output signal 3306
3318
3311
3312
Pulse Generator
3319
3316
3317
3314
Delay
fc/n
control 3320

FIG. 33A

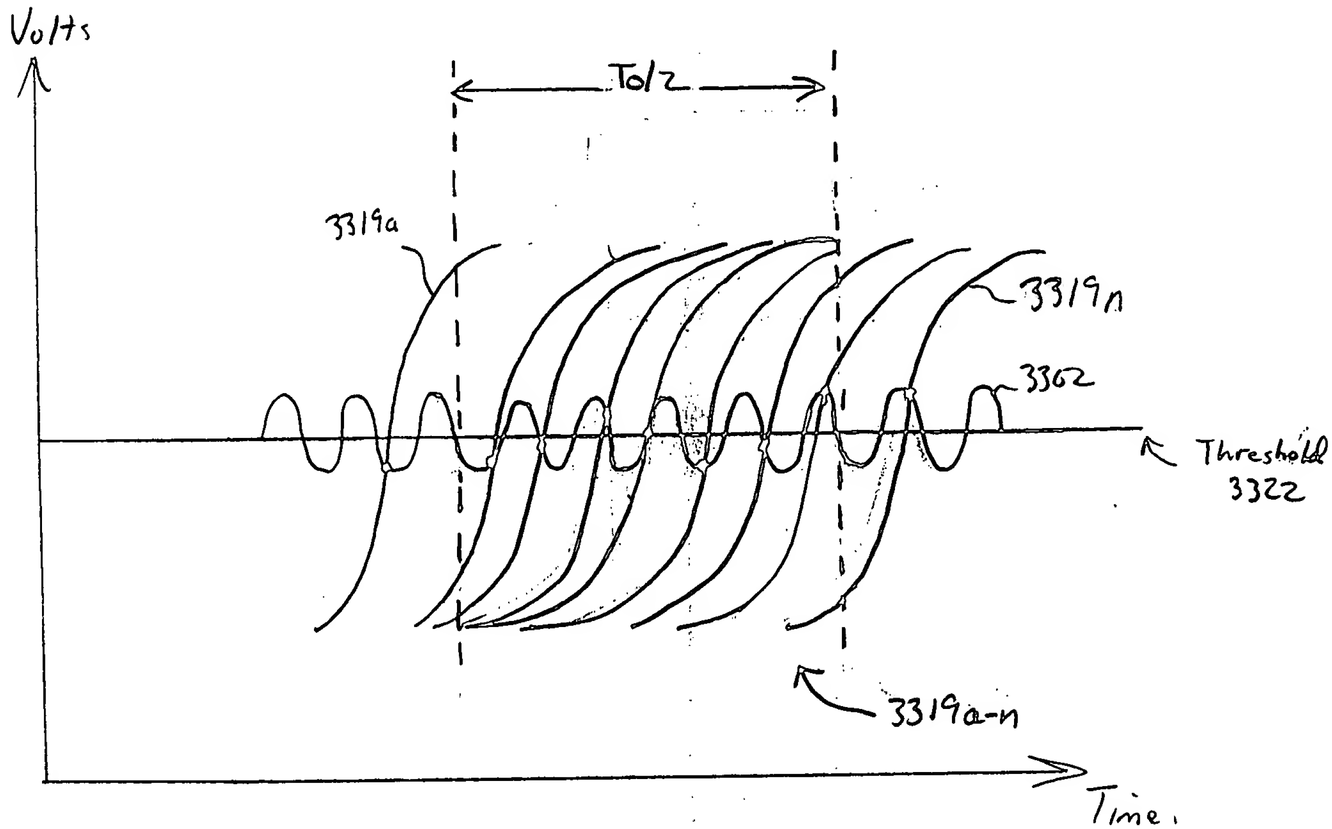
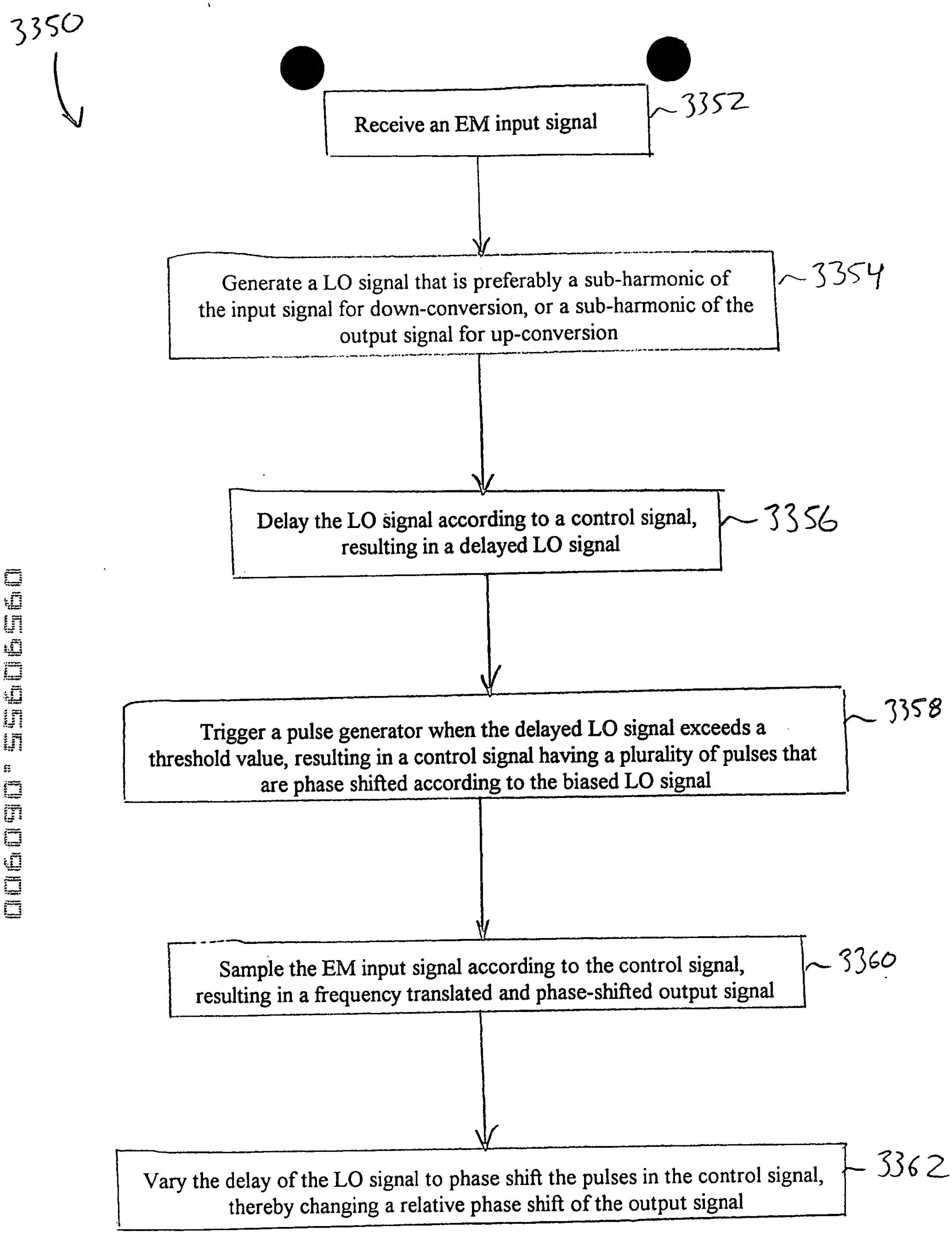


FIG. 33B



3350
Receive an EM input signal
3352
Generate a LO signal that is preferably a sub-harmonic of the input signal for down-conversion, or a sub-harmonic of the output signal for up-conversion
3354
Delay the LO signal according to a control signal, resulting in a delayed LO signal
3356
Trigger a pulse generator when the delayed LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the biased LO signal
3358
Sample the EM input signal according to the control signal, resulting in a frequency translated and phase-shifted output signal
3360
Vary the delay of the LO signal to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal
3362

FIG. 33C

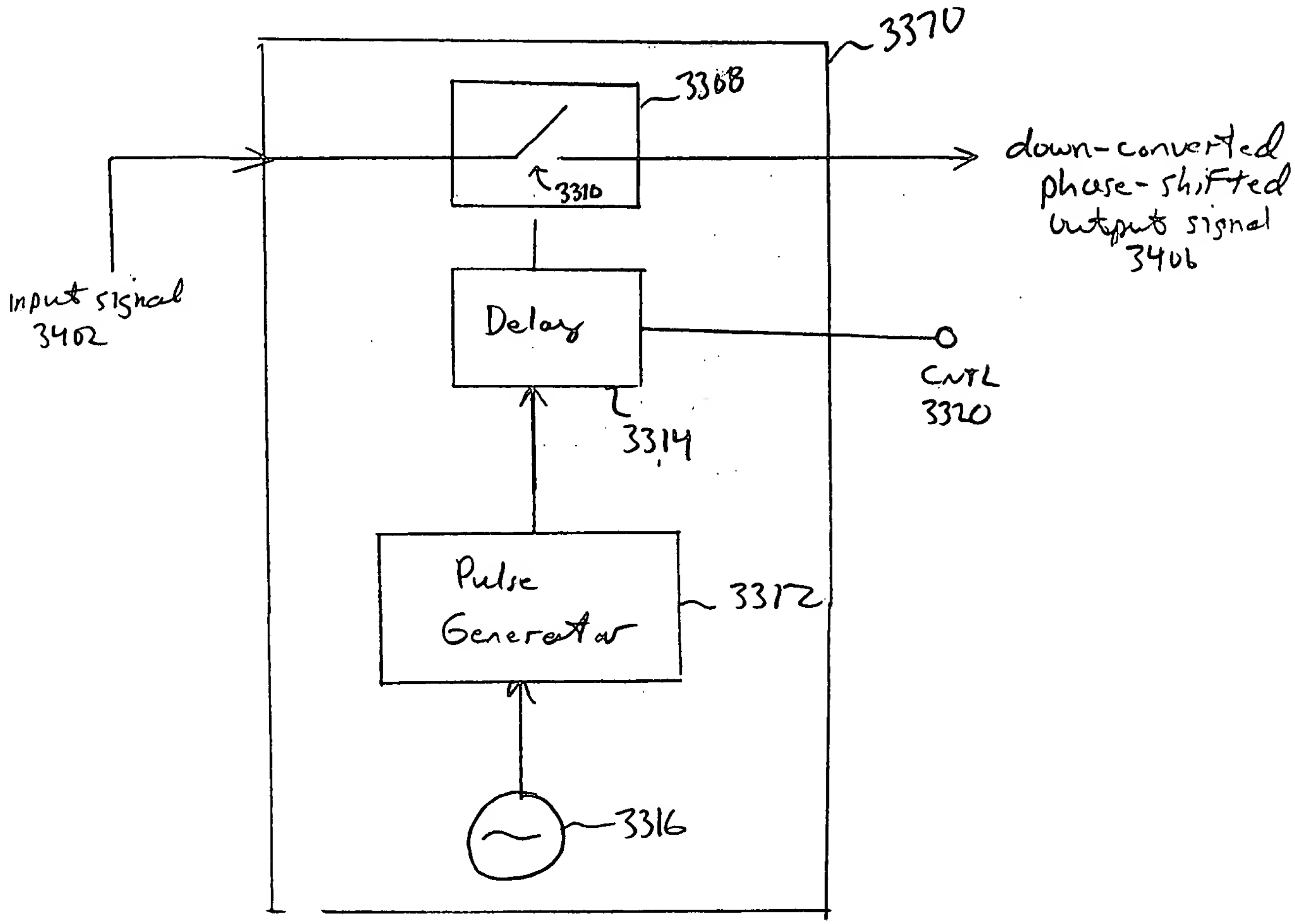

3370
3308
3310
down-converted
phase-shifted
output signal
3406
input signal
3402
Delay
3314
CNTL
3320
Pulse
Generator
3312
3316

FIG. 33D

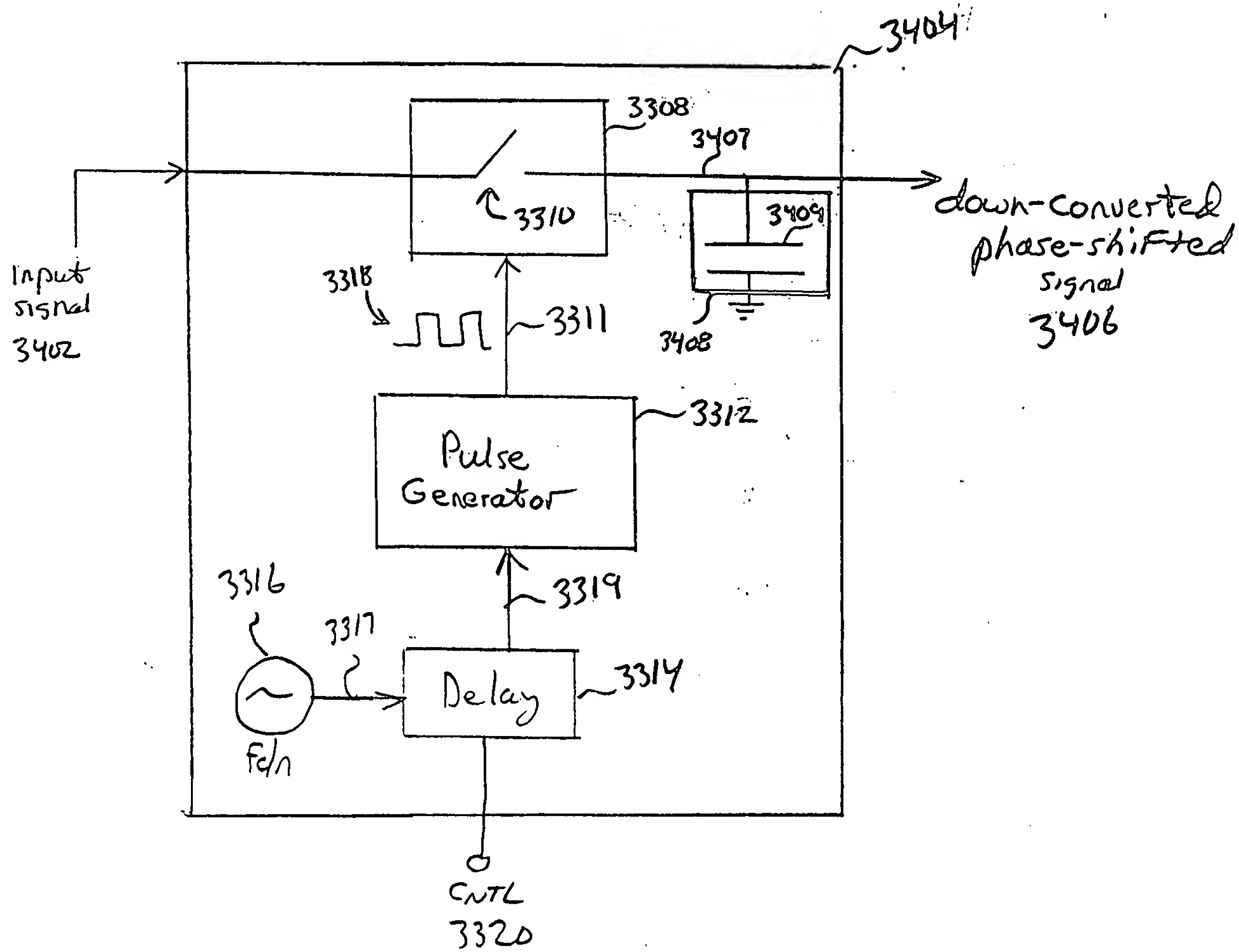
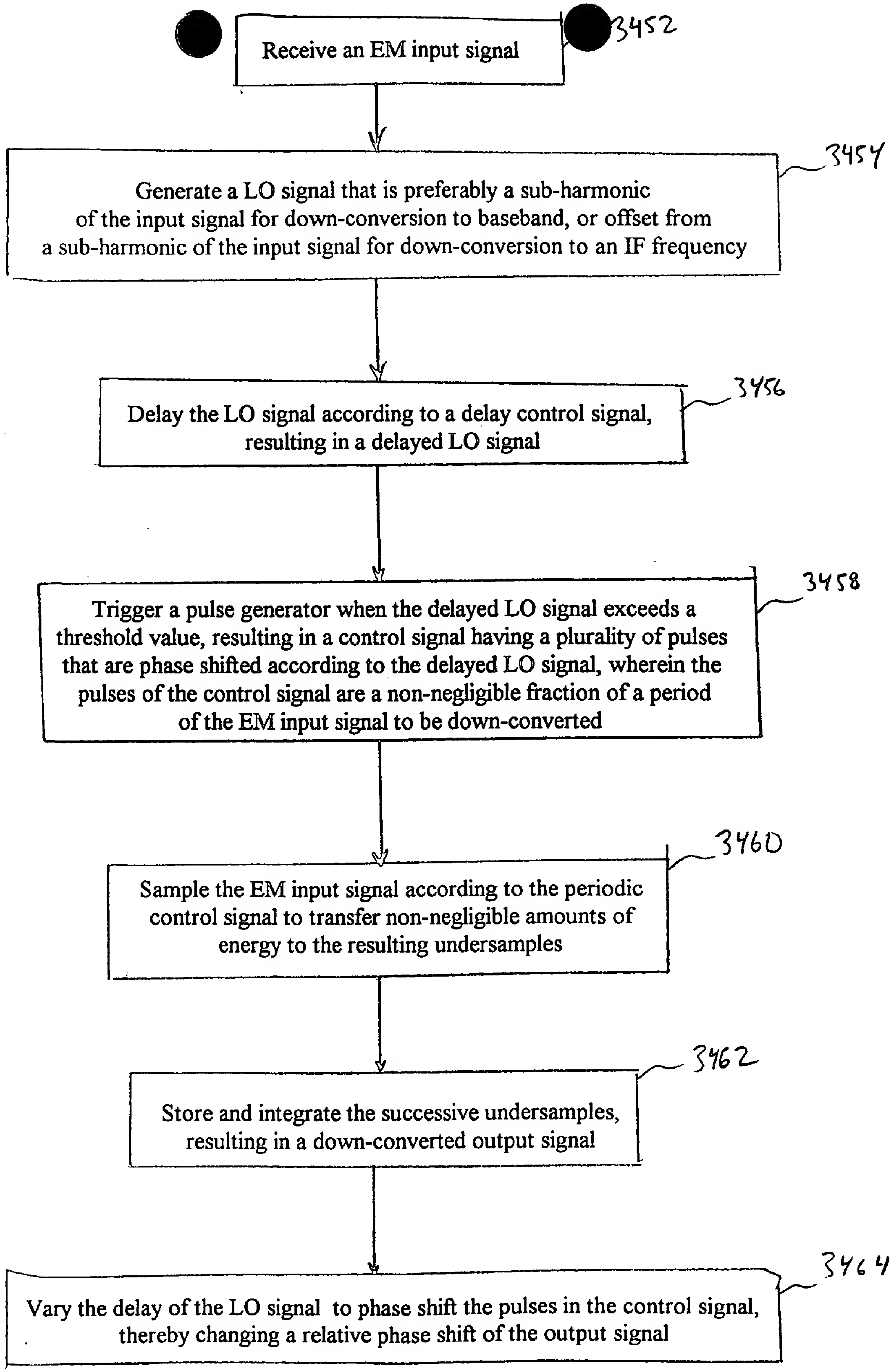

3404
3308
3407
3310
3409
down-converted phase-shifted signal 3406
input signal 3402
3318
3311
3408
3312
Pulse Generator
3319
3316
3317
Delay
3314
Fc/n
CNTL 3320

FIG. 34A



Receive an EM input signal
3452
Generate a LO signal that is preferably a sub-harmonic of the input signal for down-conversion to baseband, or offset from a sub-harmonic of the input signal for down-conversion to an IF frequency
3454
Delay the LO signal according to a delay control signal, resulting in a delayed LO signal
3456
Trigger a pulse generator when the delayed LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the delayed LO signal, wherein the pulses of the control signal are a non-negligible fraction of a period of the EM input signal to be down-converted
3458
Sample the EM input signal according to the periodic control signal to transfer non-negligible amounts of energy to the resulting undersamples
3460
Store and integrate the successive undersamples, resulting in a down-converted output signal
3462
Vary the delay of the LO signal to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal
3464

FIG. 34B

09560955 . 060900

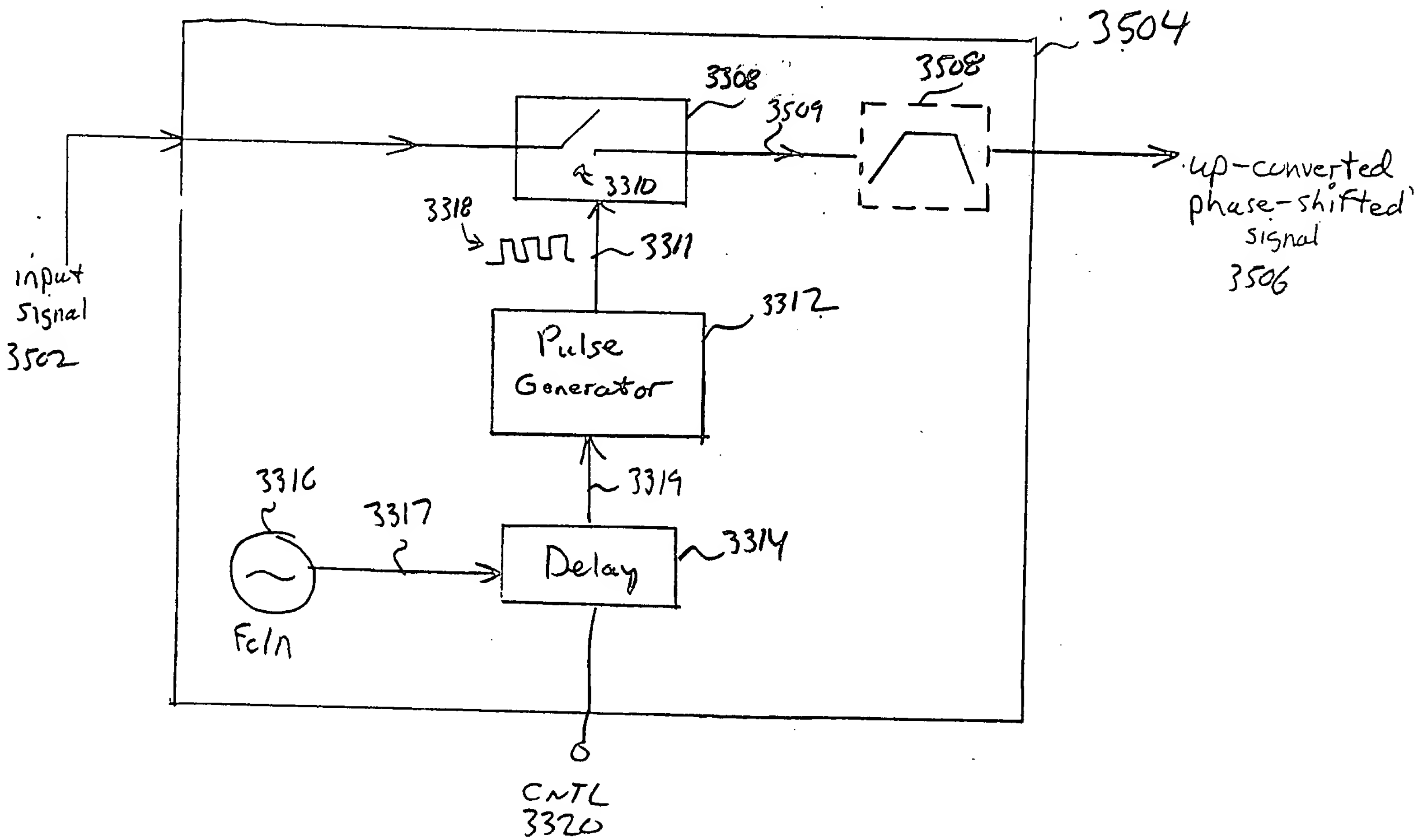


FIG. 35A

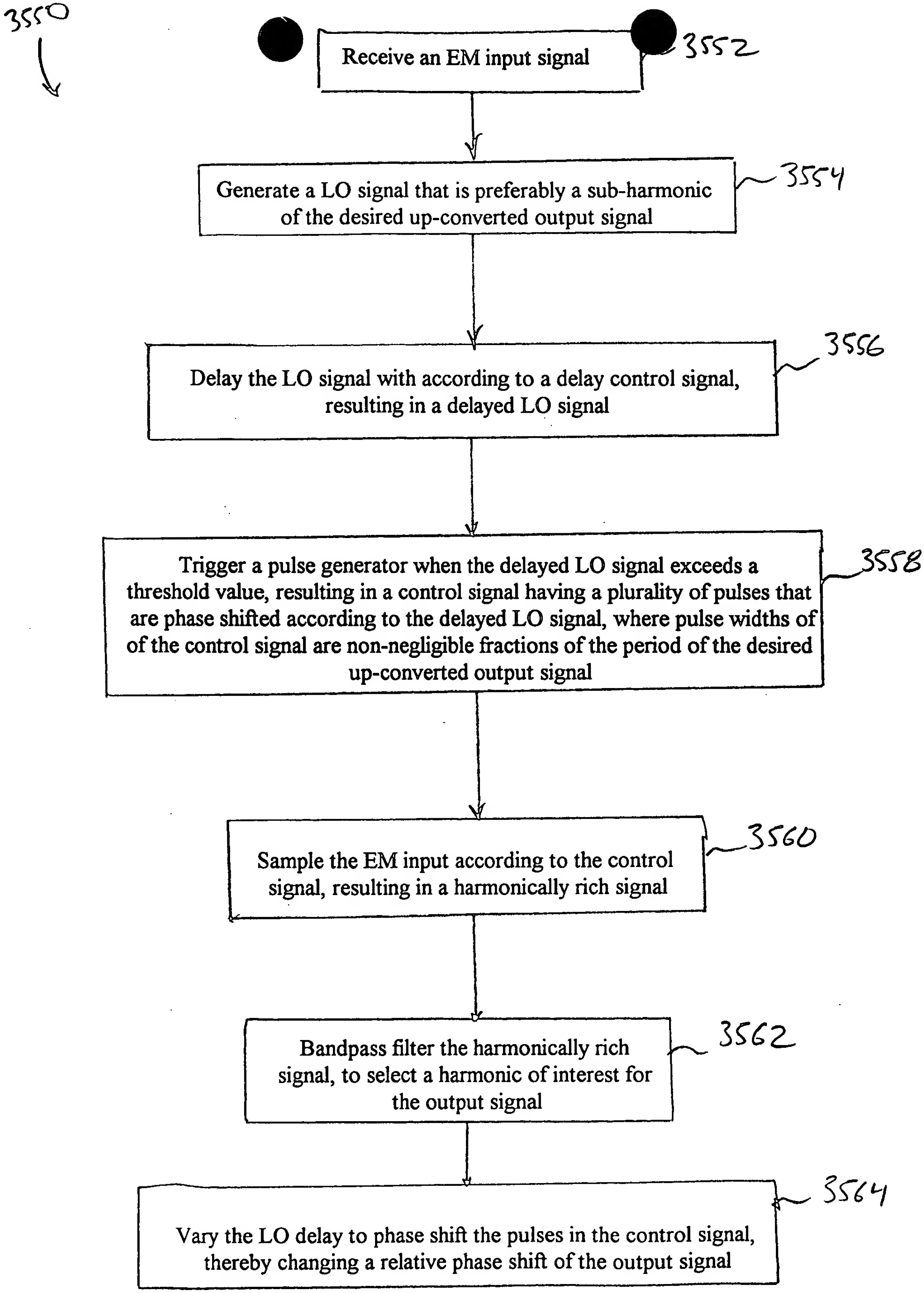

3550
Receive an EM input signal
3552
Generate a LO signal that is preferably a sub-harmonic of the desired up-converted output signal
3554
Delay the LO signal with according to a delay control signal, resulting in a delayed LO signal
3556
Trigger a pulse generator when the delayed LO signal exceeds a threshold value, resulting in a control signal having a plurality of pulses that are phase shifted according to the delayed LO signal, where pulse widths of of the control signal are non-negligible fractions of the period of the desired up-converted output signal
3558
Sample the EM input according to the control signal, resulting in a harmonically rich signal
3560
Bandpass filter the harmonically rich signal, to select a harmonic of interest for the output signal
3562
Vary the LO delay to phase shift the pulses in the control signal, thereby changing a relative phase shift of the output signal
3564

FIG. 35B

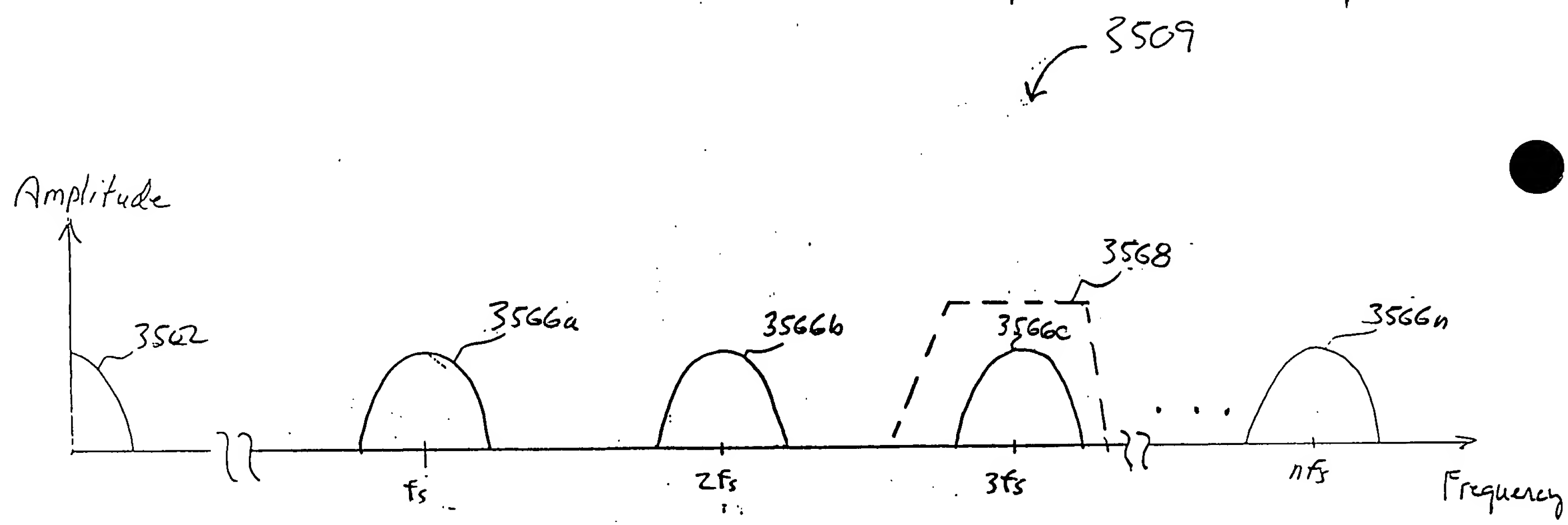

3509
Amplitude
3562
3566a
3566b
3568
3566c
3566n
fs
2fs
3fs
nfs
Frequency

FIG. 35C

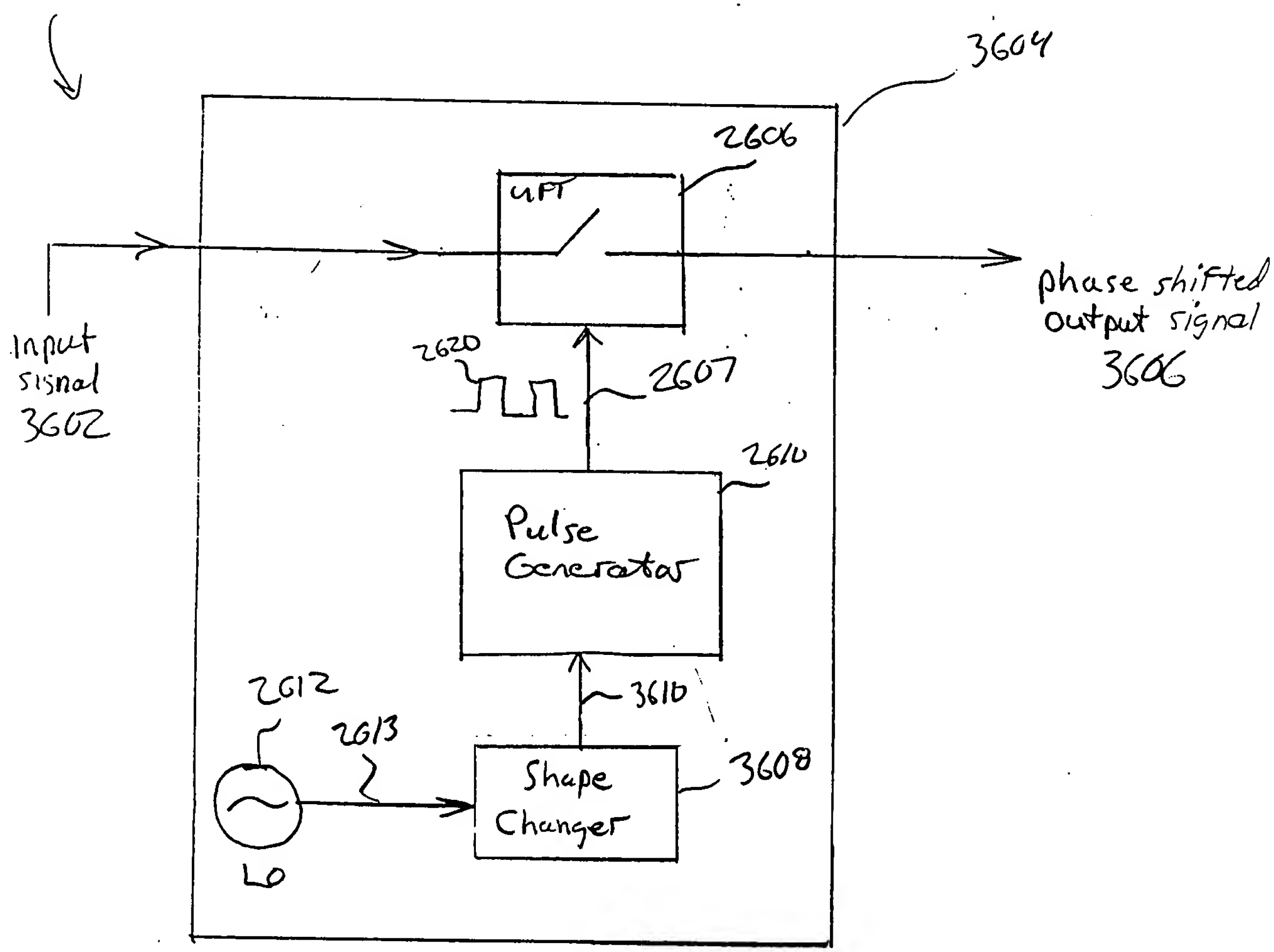

3604
2606
UFT
Input signal 3602
phase shifted output signal 3606
2620
2607
2610
Pulse Generator
2612
2613
3610
3608
Shape Changer
LO

FIG. 36

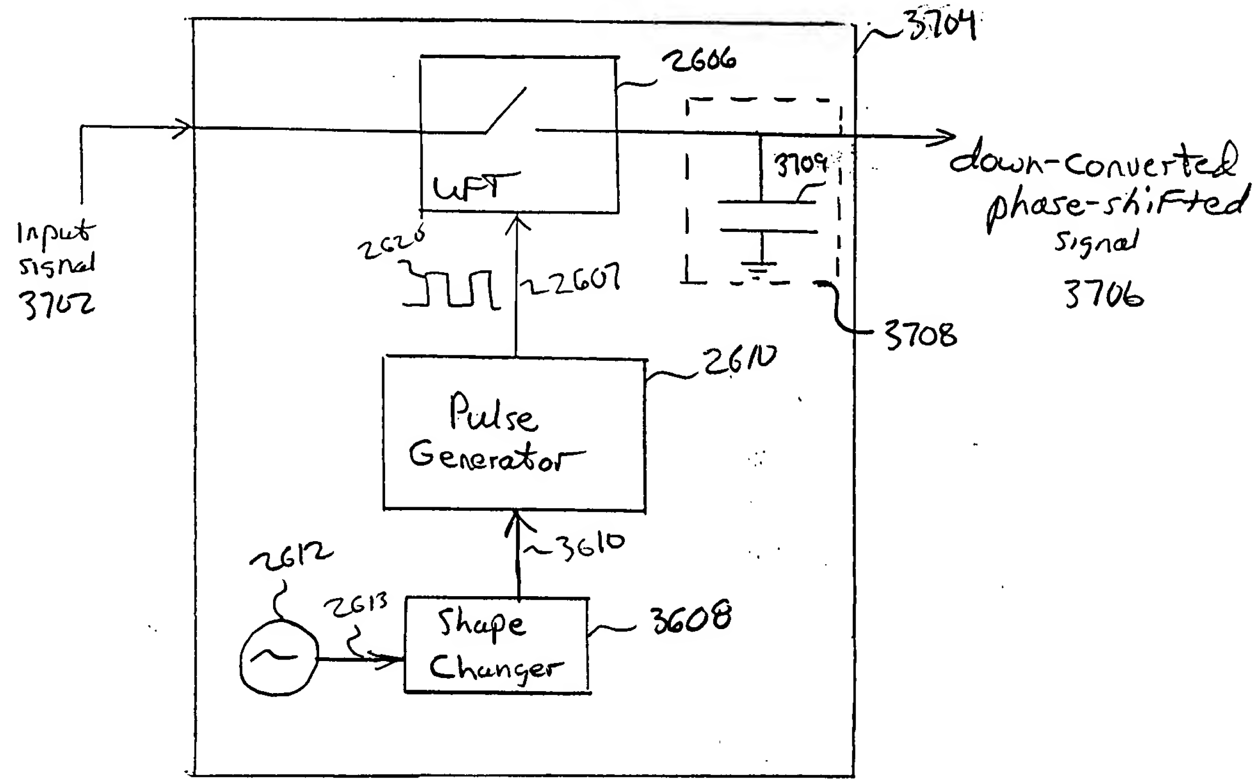

3704
2606
WFT
3709
down-converted
phase-shifted
signal
3706
Input
signal
3702
2626
2607
3708
2610
Pulse
Generator
3610
2612
2613
Shape
Changer
3608

FIG. 37

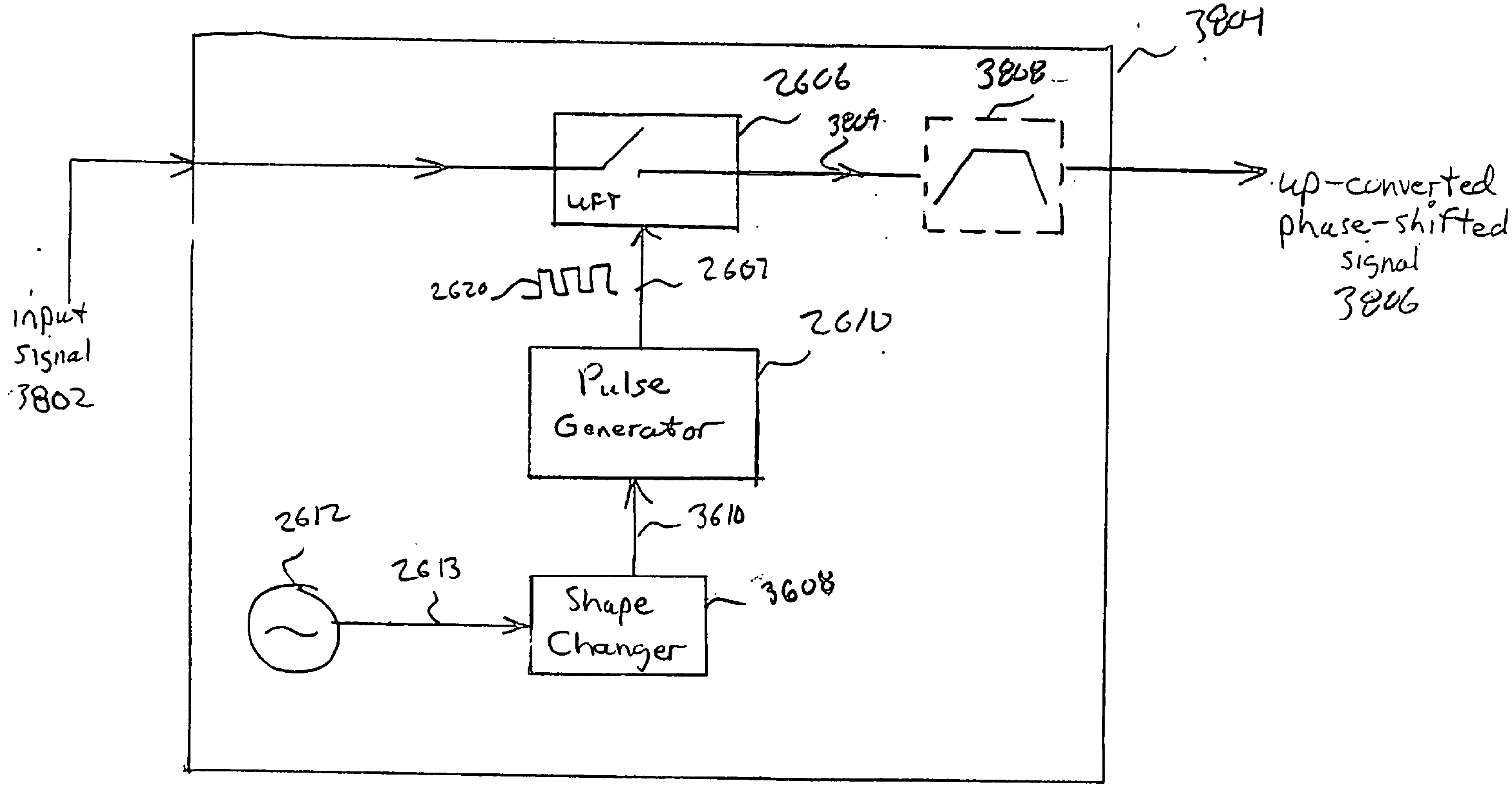

3804
2606
3808
3804
UFT
input signal 3802
2620
2607
2610
Pulse Generator
3610
2612
2613
3608
Shape Changer
up-converted phase-shifted signal 3806

FIG. 38

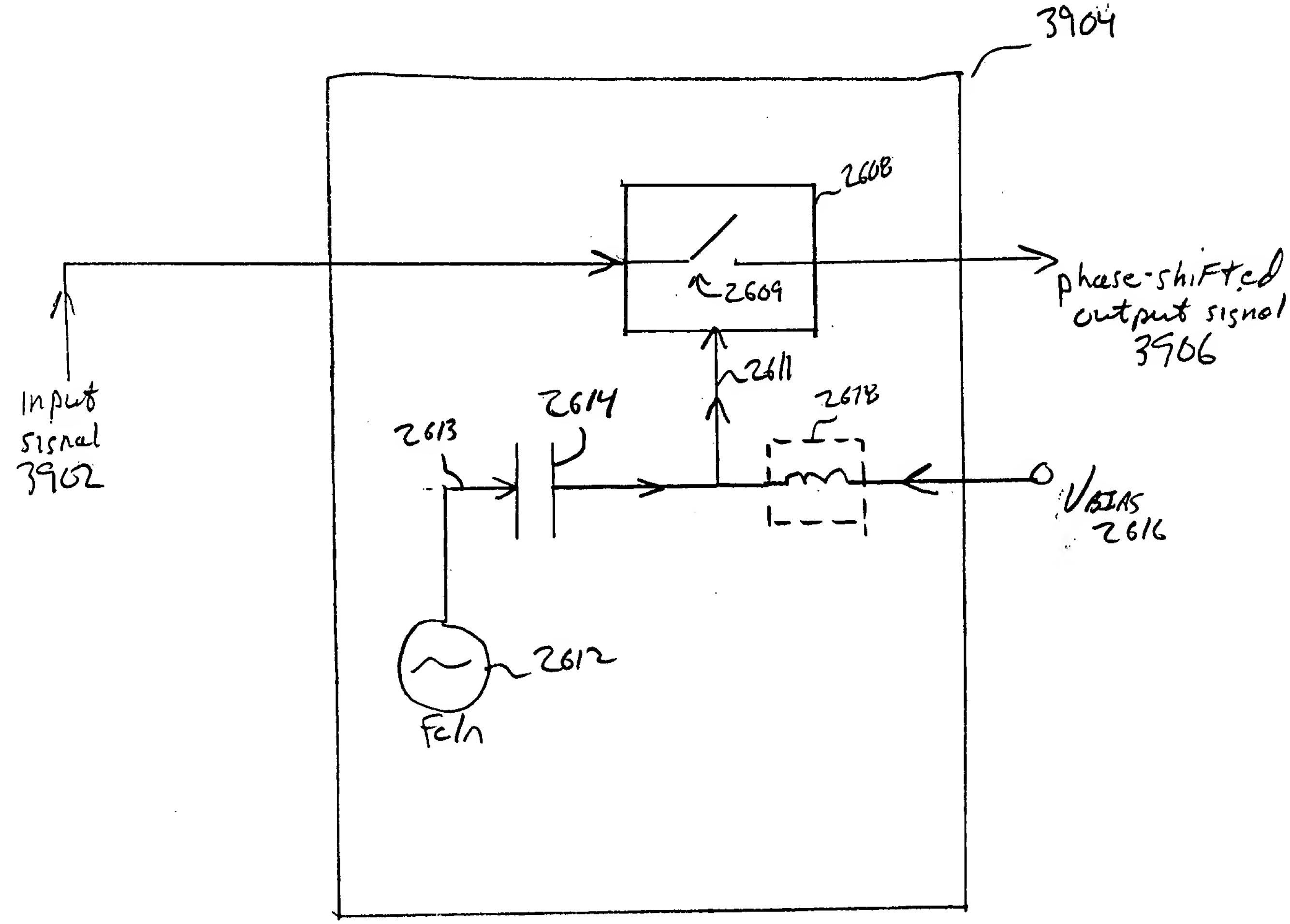

3904
2608
2609
phase-shifted output signal 3906
2611
2618
input signal 3902
2613
2614
V_{BIAS} 2616
2612
Fc/n

FIG. 39

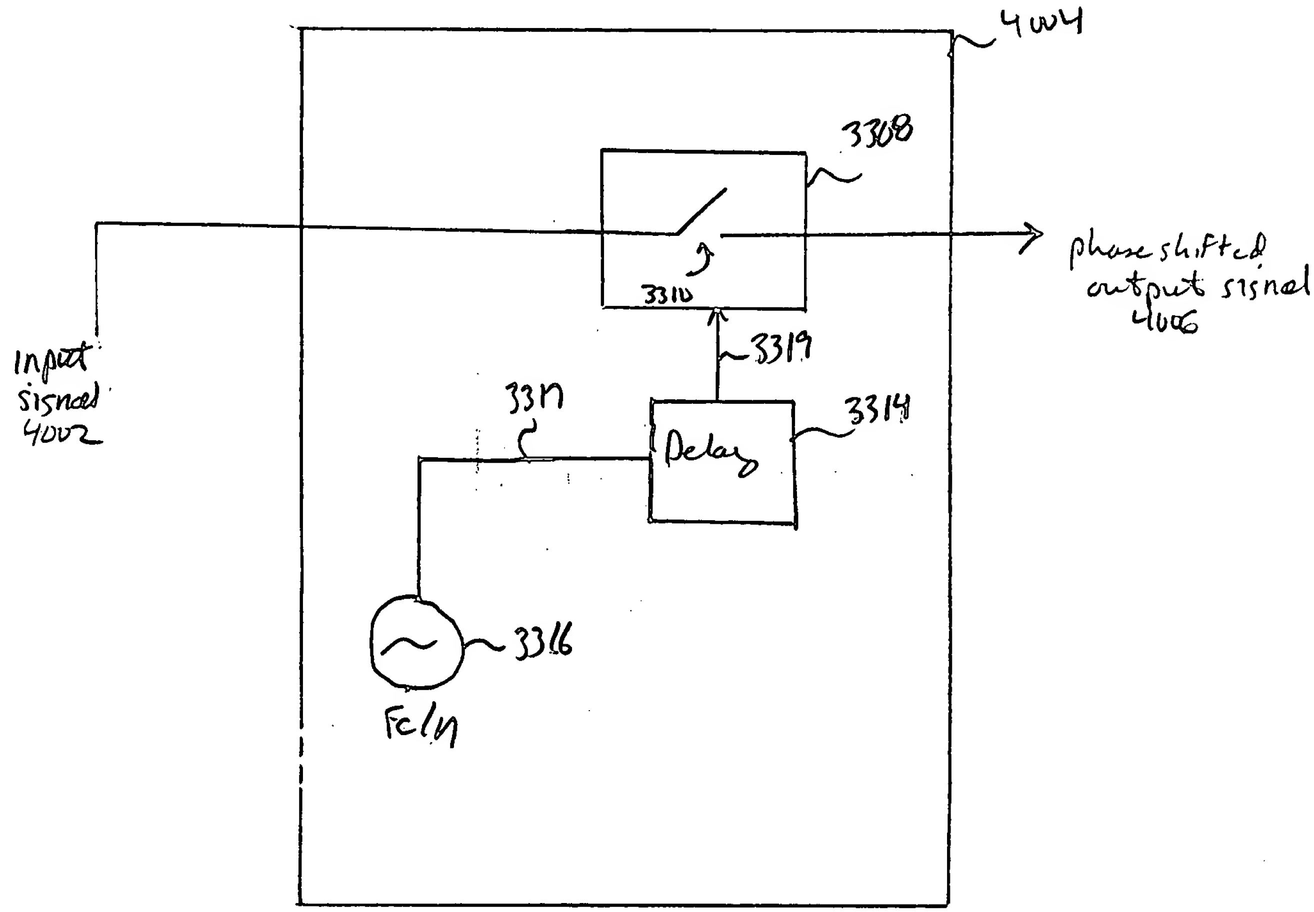

4004
3308
phase shifted
output signal
4006
3310
3319
input
signal
4002
3317
3314
Delay
3316
Fc/n

FIG. 4D

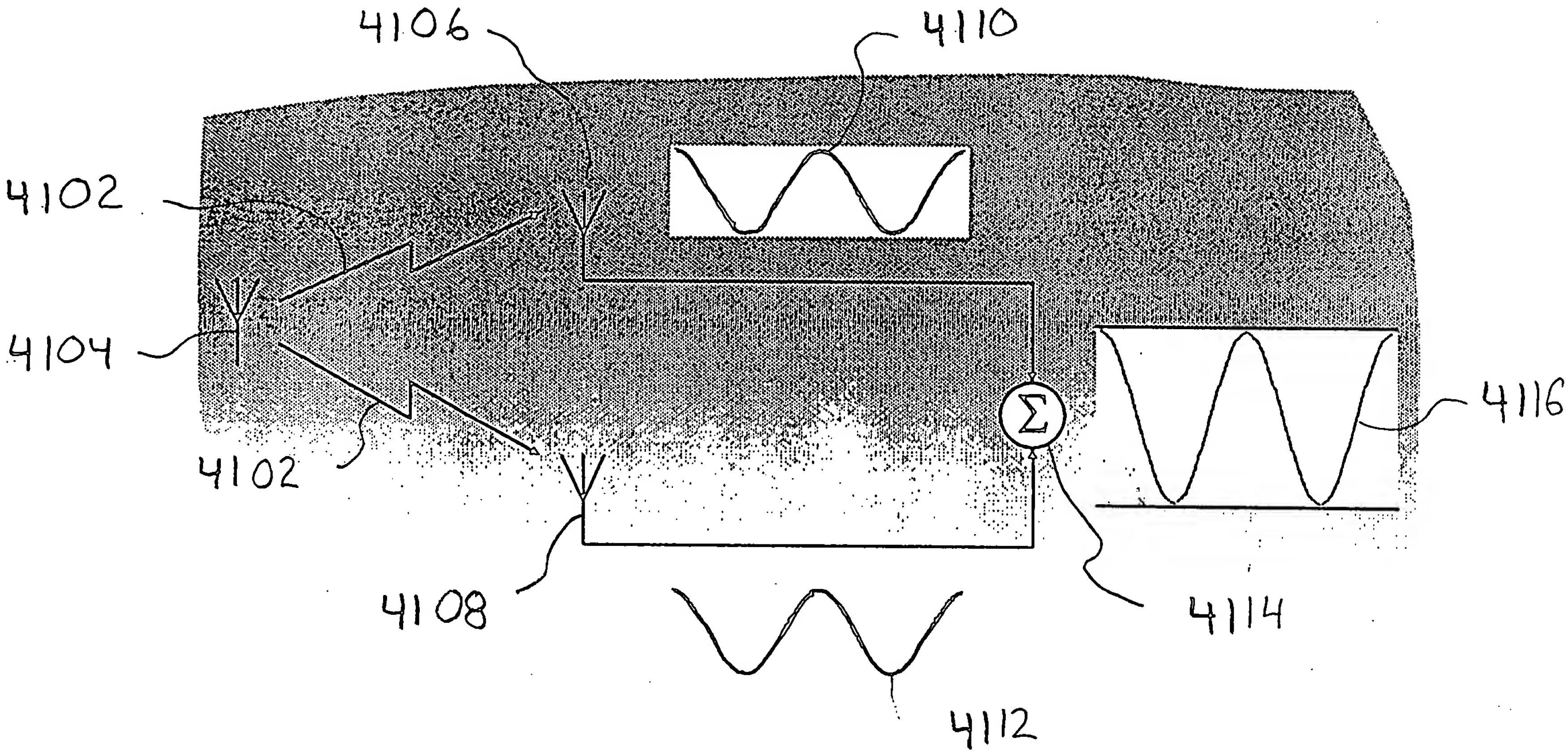


FIG. 41

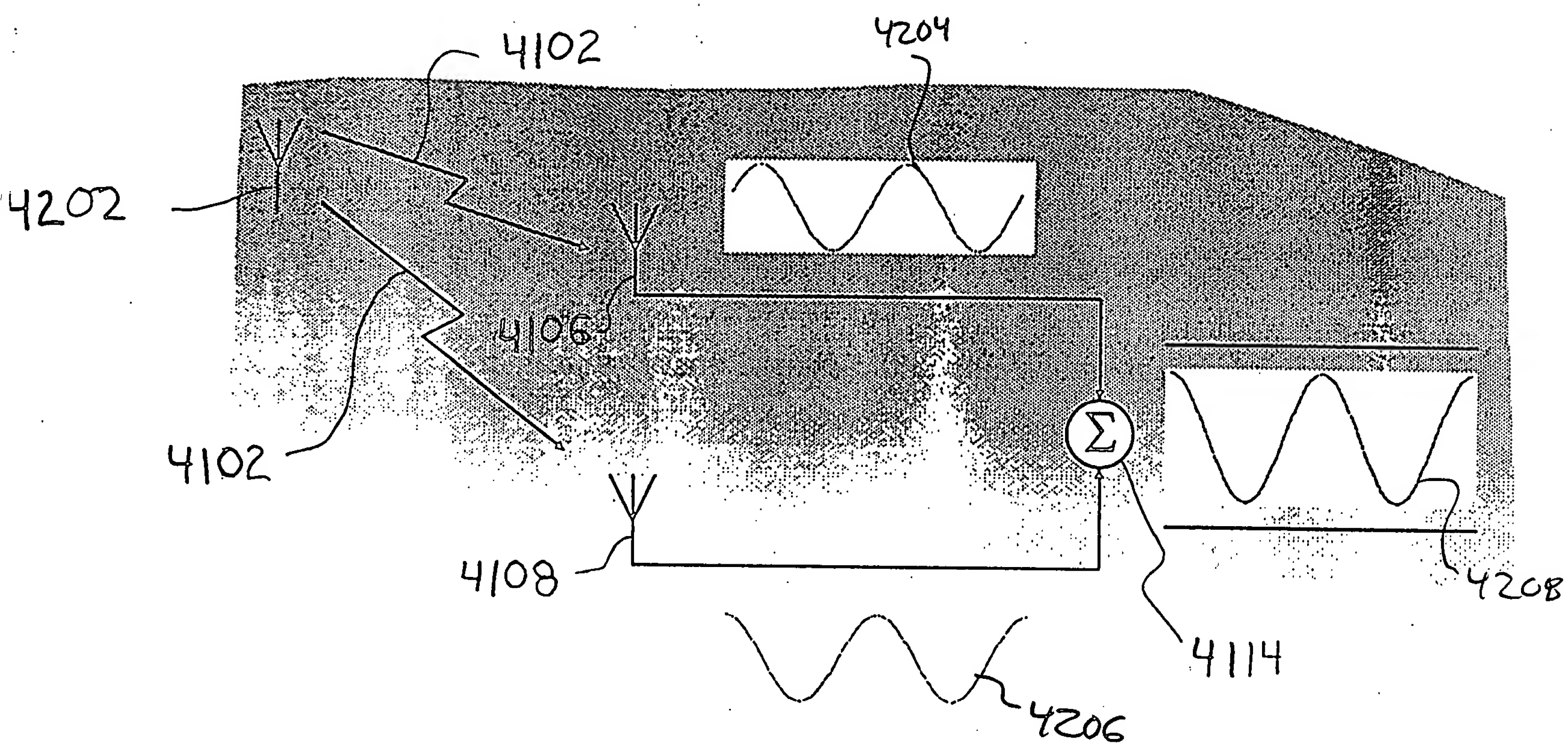


FIG. 42

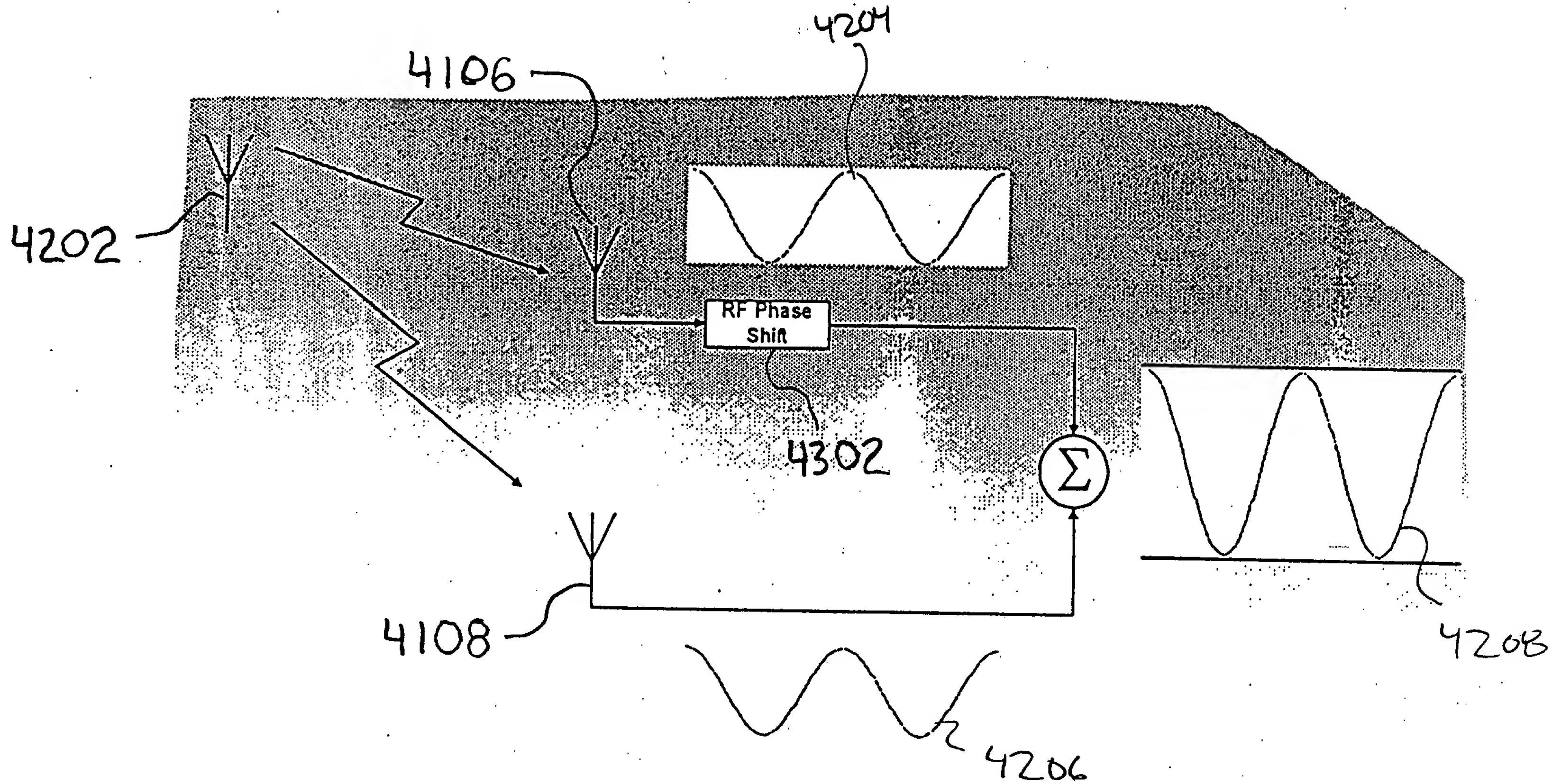


FIG. 43

No RF Phase Shift

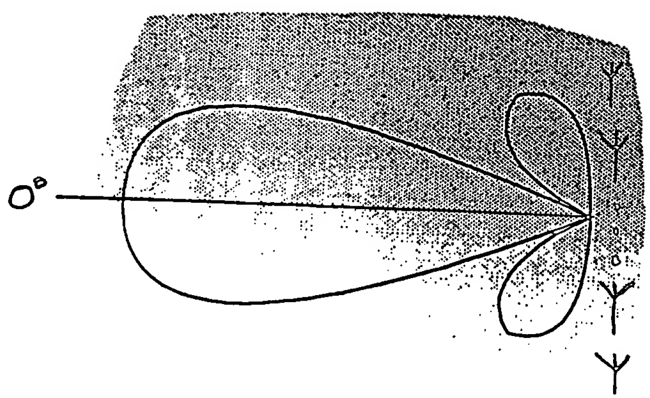


FIG. 44A

RF Phase Shift

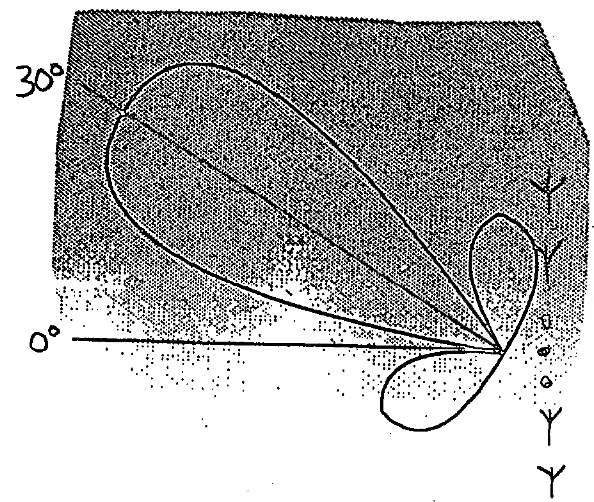


FIG. 44B

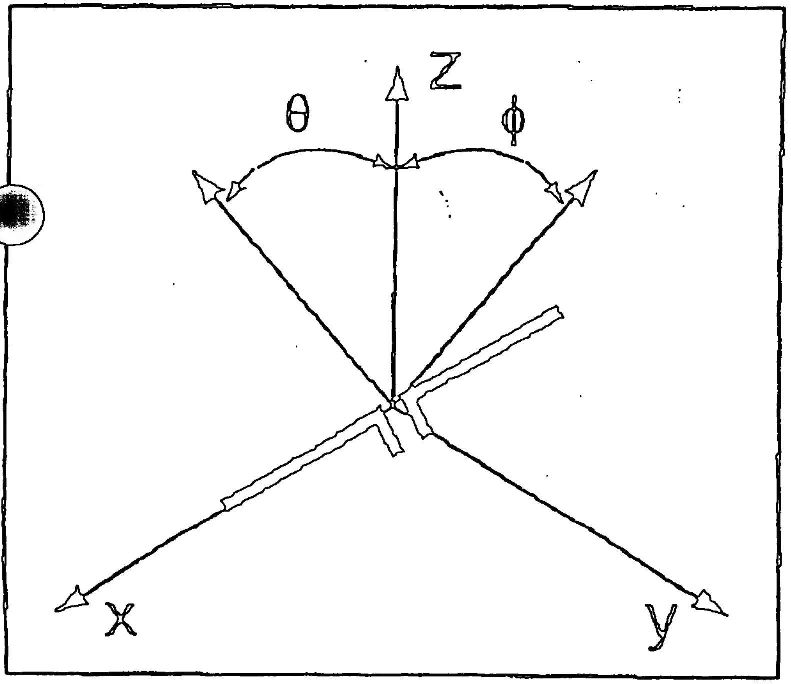


FIG. 45A *Half-wave dipole*

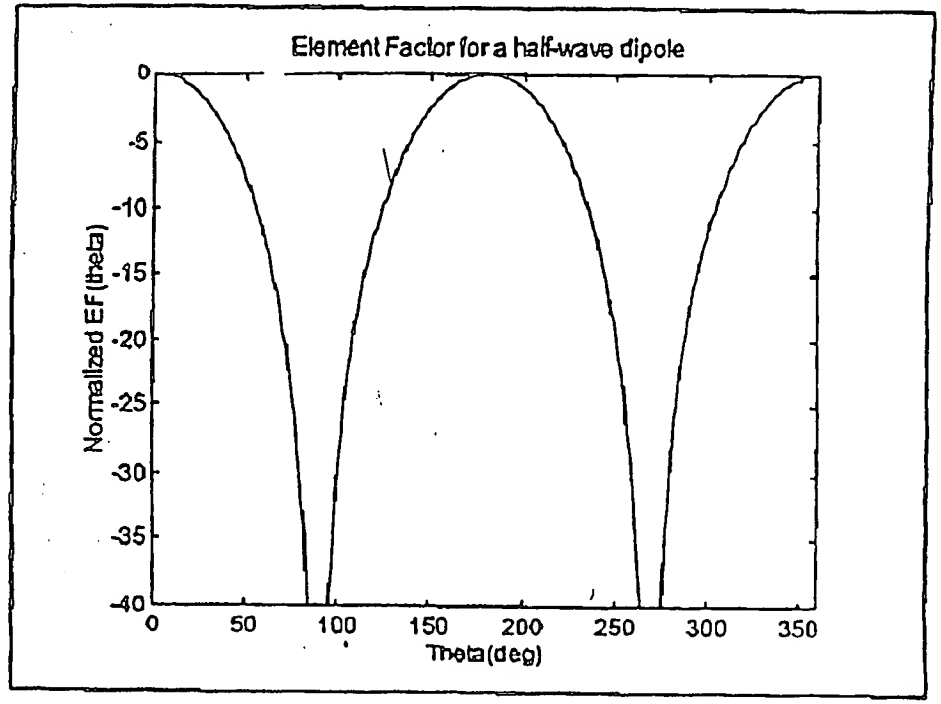


FIG. 45B *E-plane element factor for a half-wave dipole.*

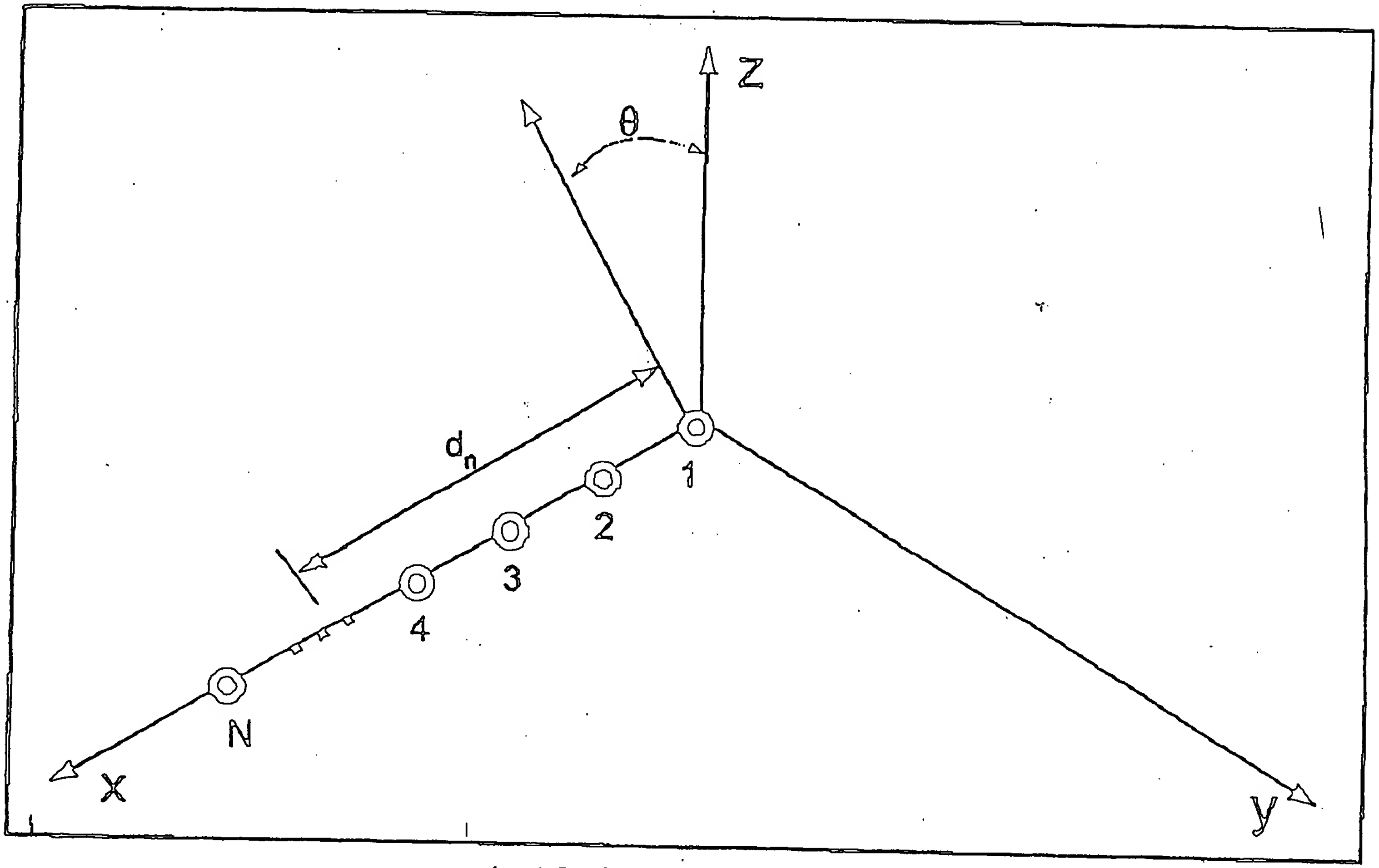


FIG. 46 *An N-element linear antenna array.*

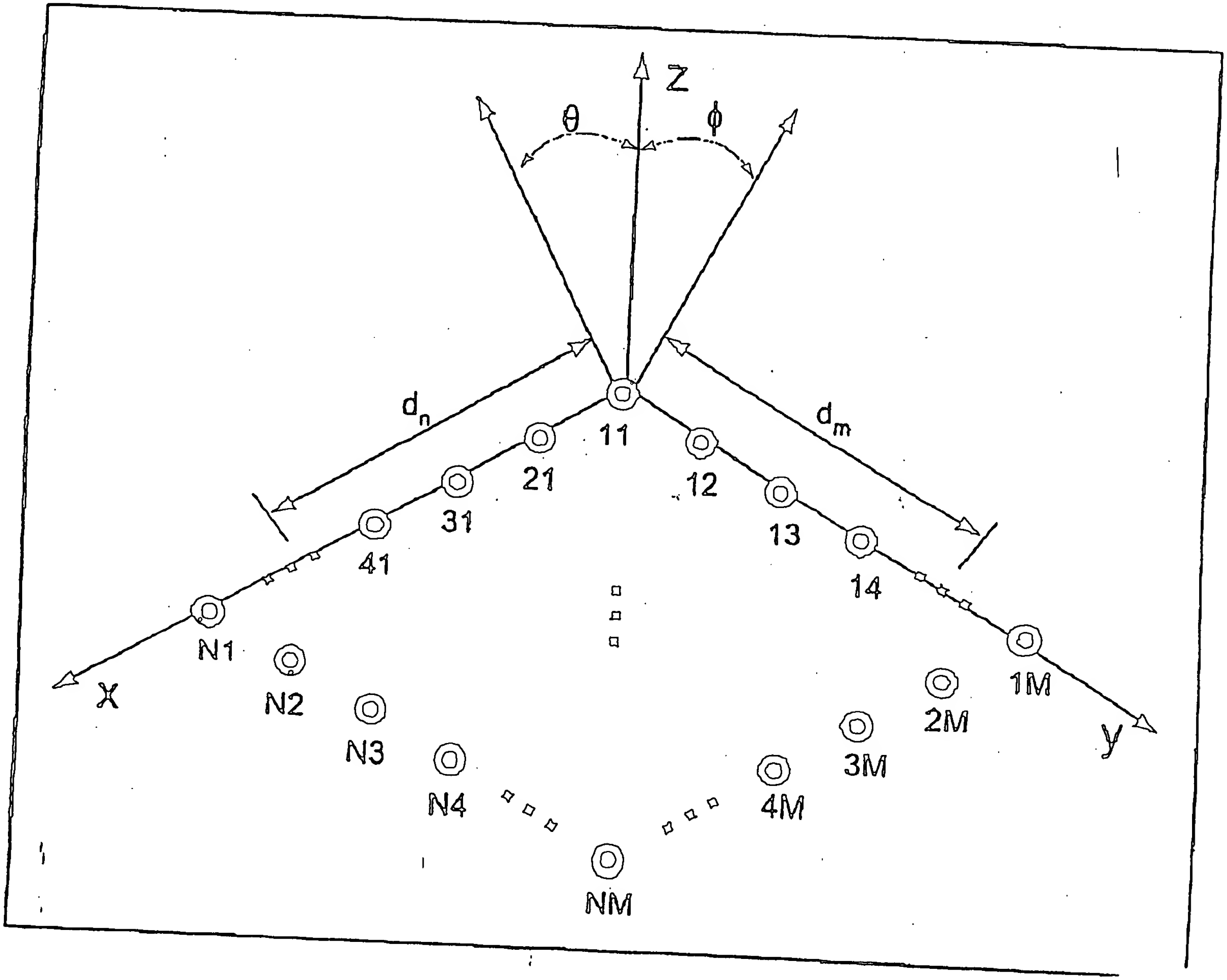


FIG. 47

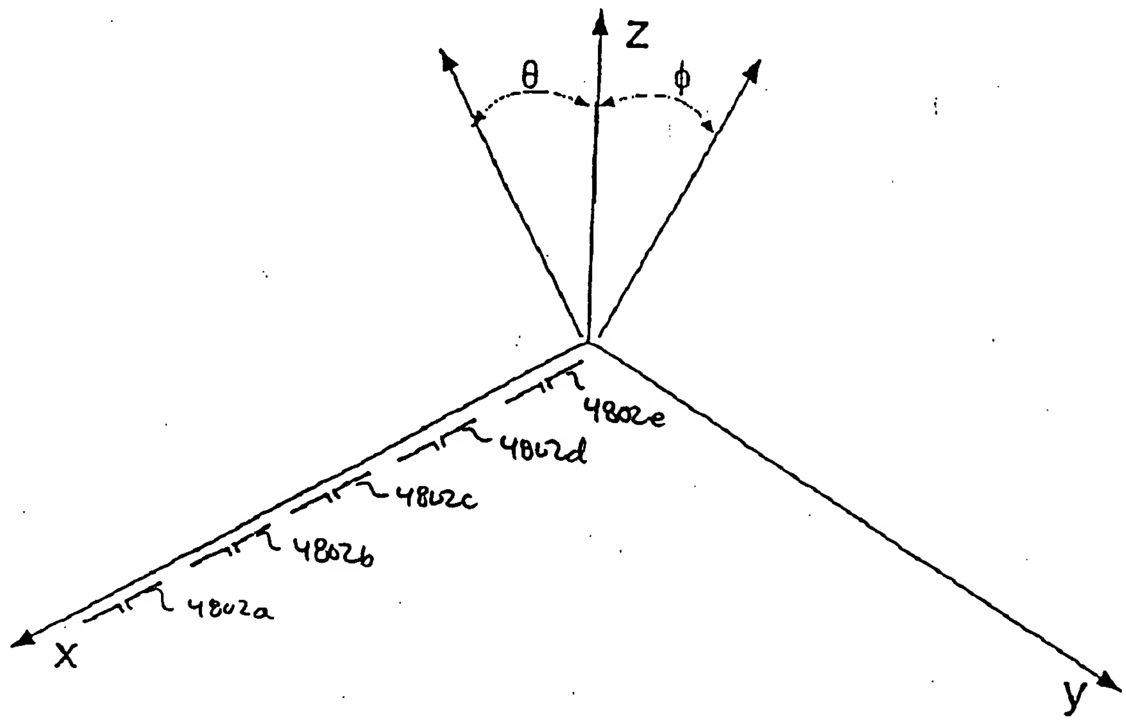


FIG. 48 *A linear array of five half wave dipoles.*

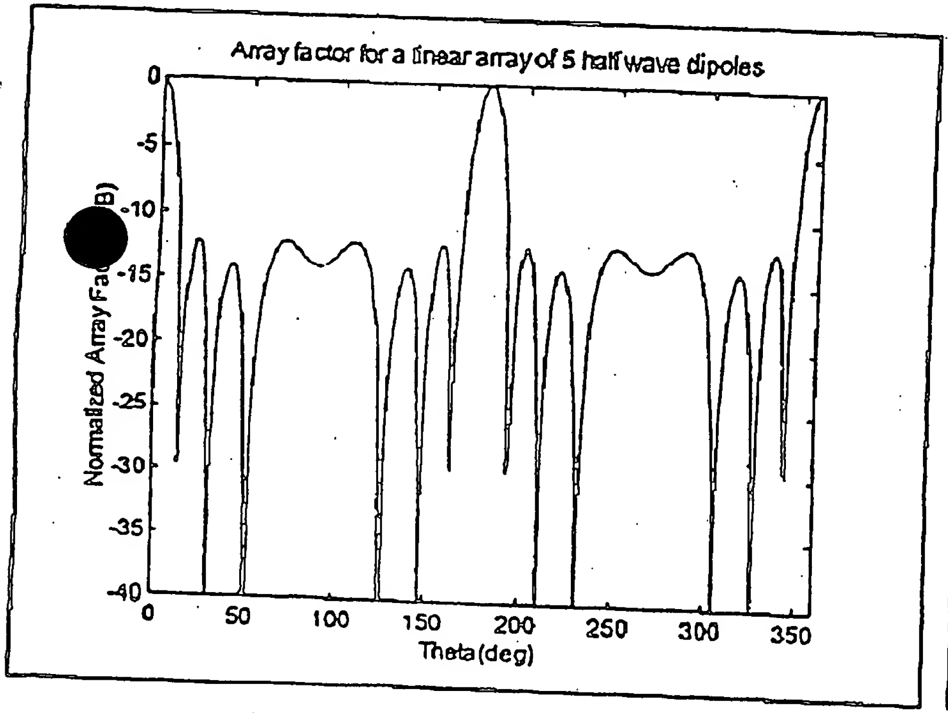


FIG. 49A Array factor for the linear array.

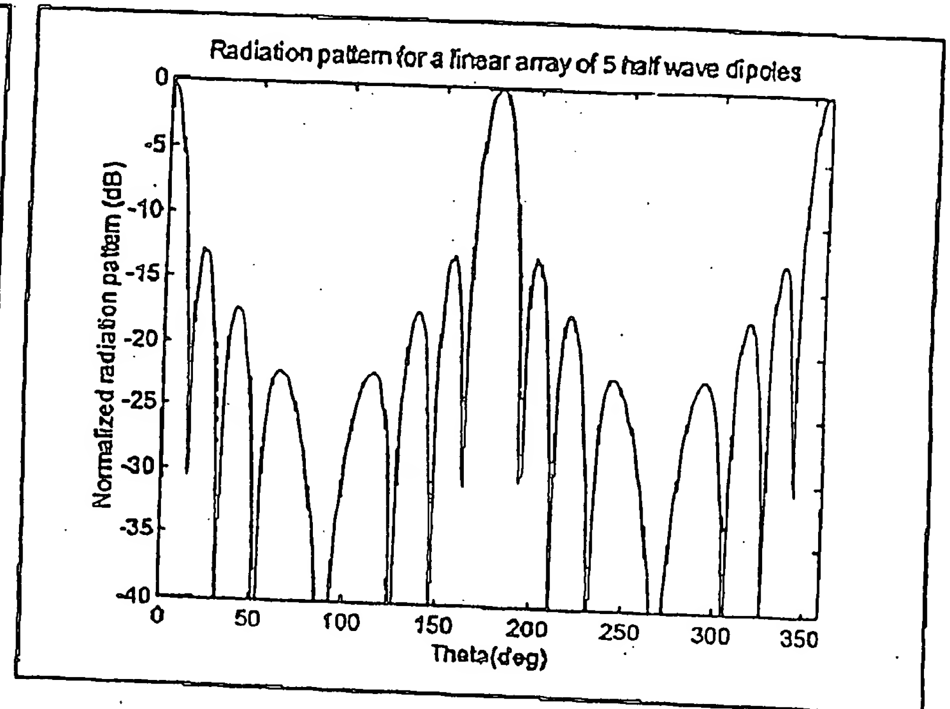


FIG.49B Radiation pattern for the linear array.

09590955 .060900

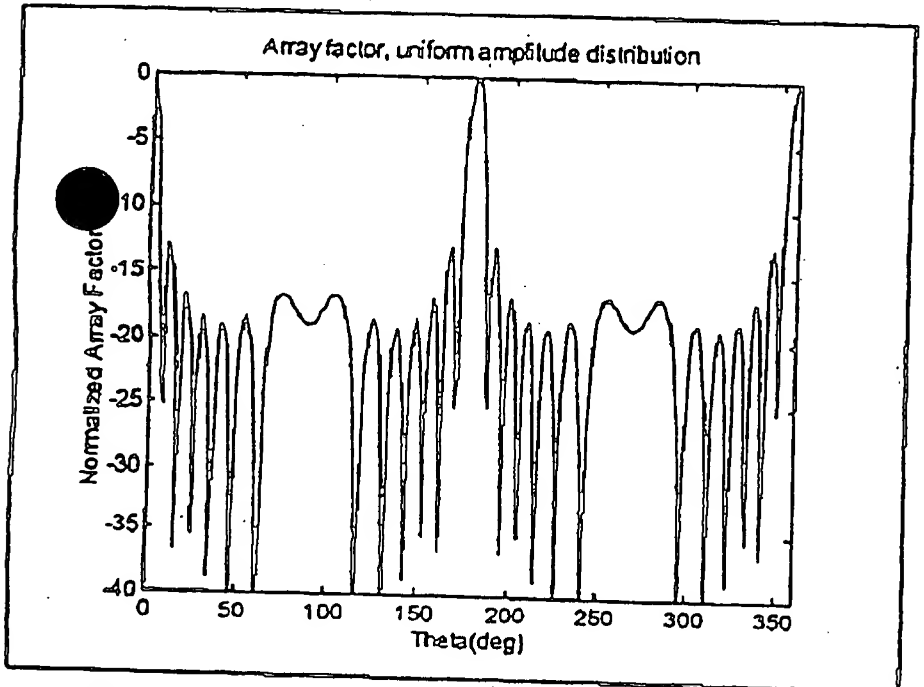


FIG. 50A Array factor, uniform amplitude distribution

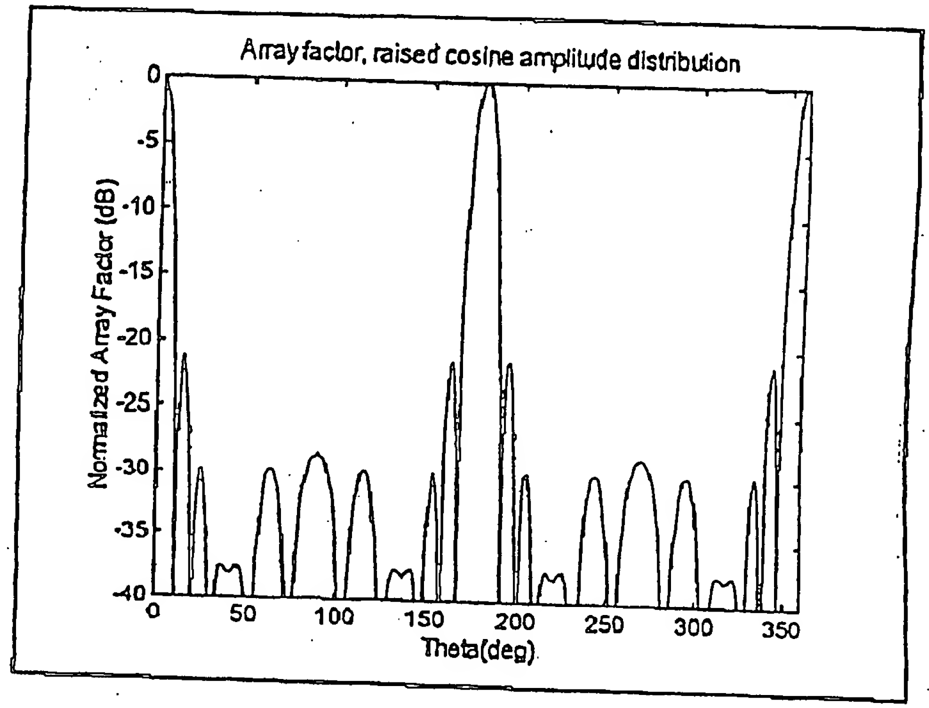


FIG. 50B Array factor raised cosine amplitude distribution

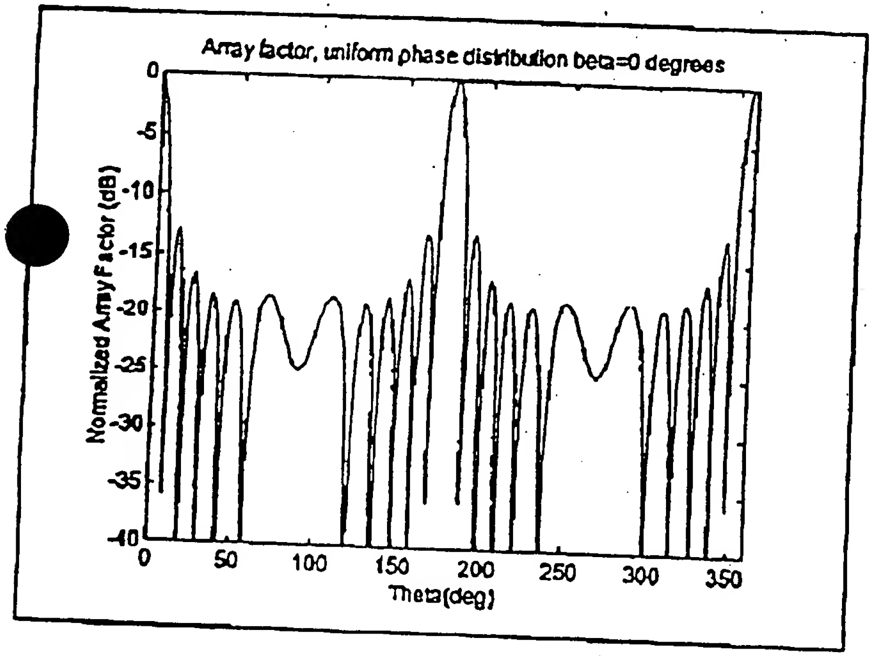


FIG. 51A *Array factor, uniform phase distribution*

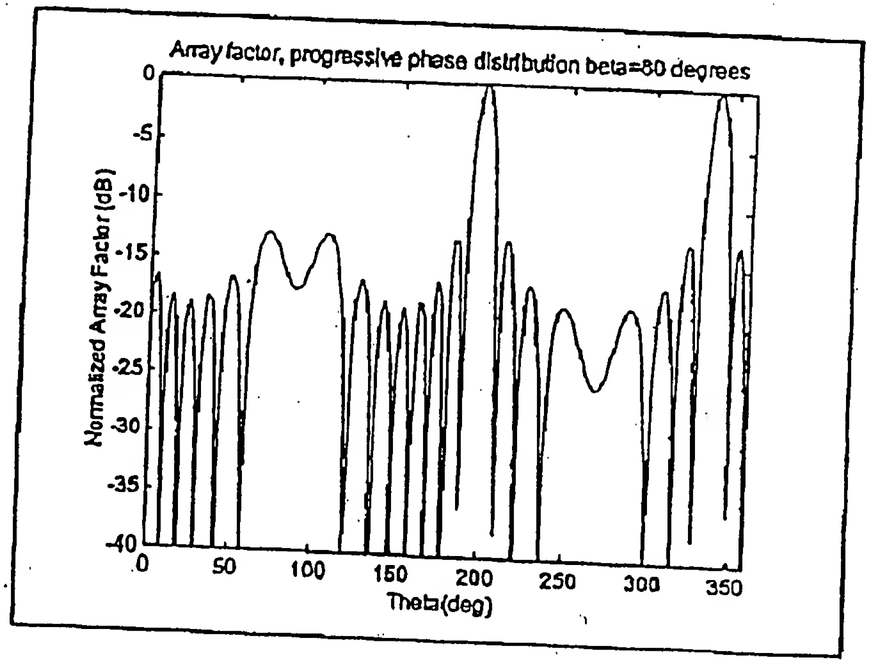


FIG. 51B *Array factor progressive phase distribution*

00609055606560

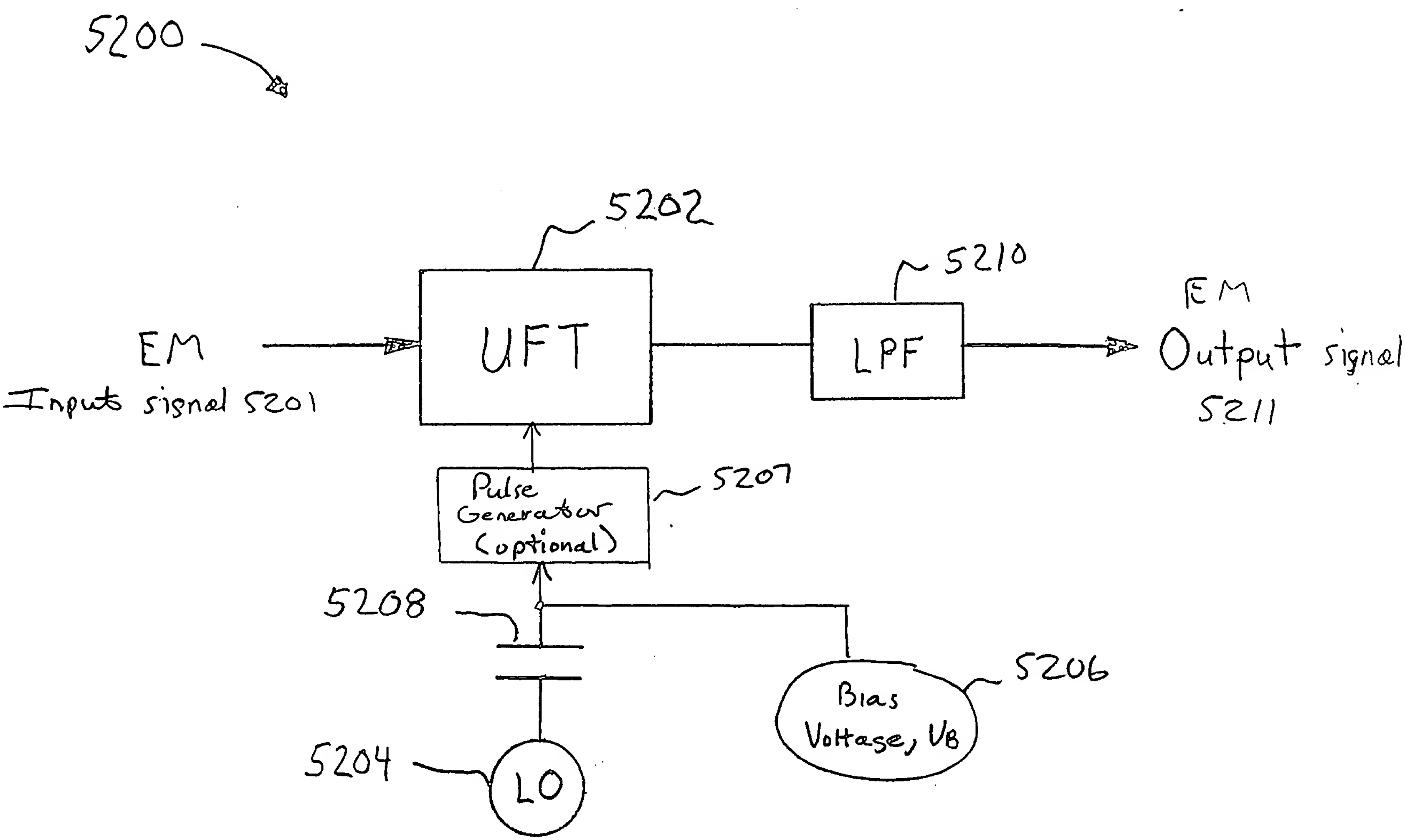


FIG. 52

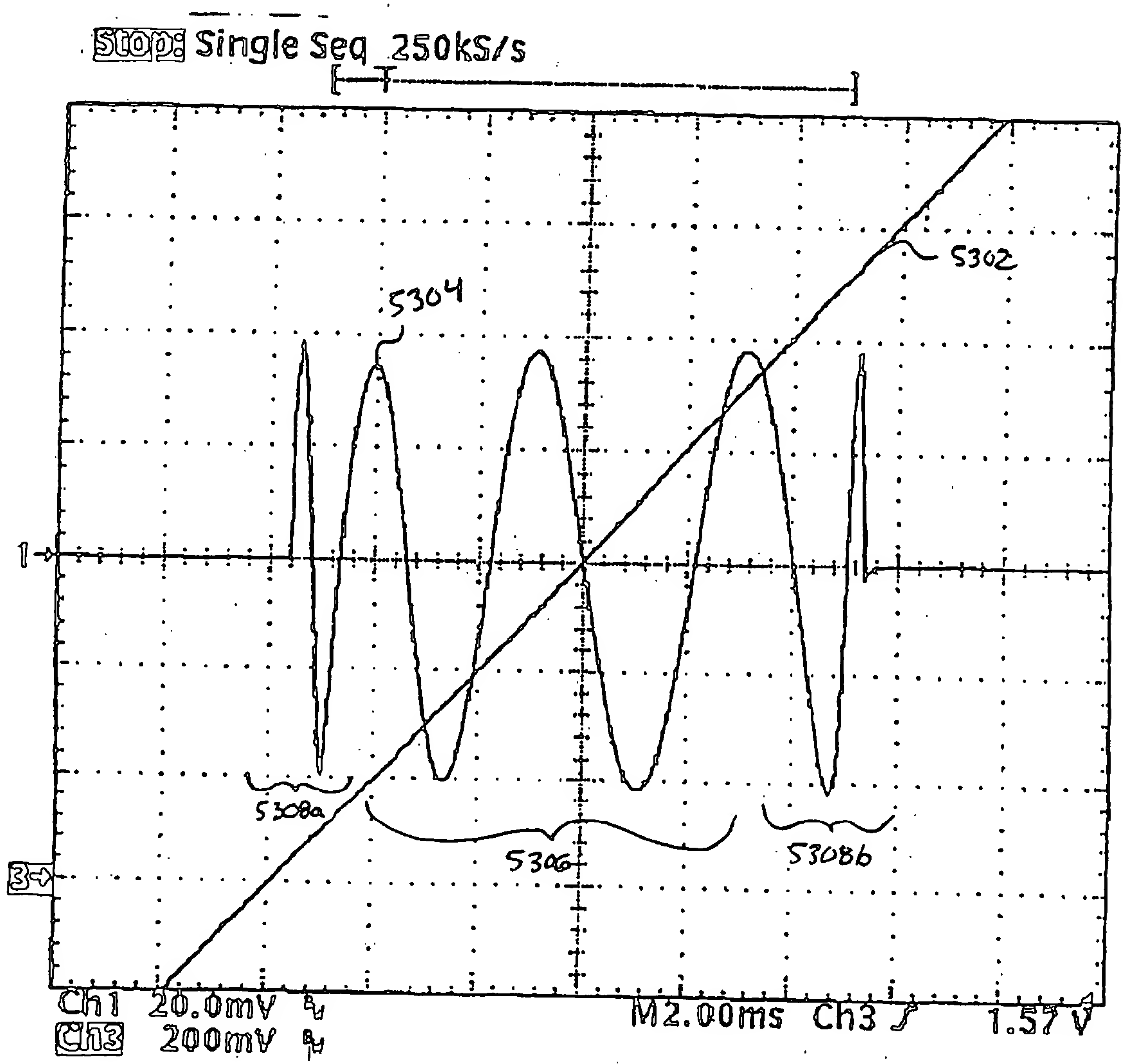

Stop: Single Seq 250kS/s
5304
5302
1→
3→
5308a
5306
5308b
Ch1 20.0mV
Ch3 200mV
M2.00ms Ch3 ∫ 1.57 V

FIG. 53

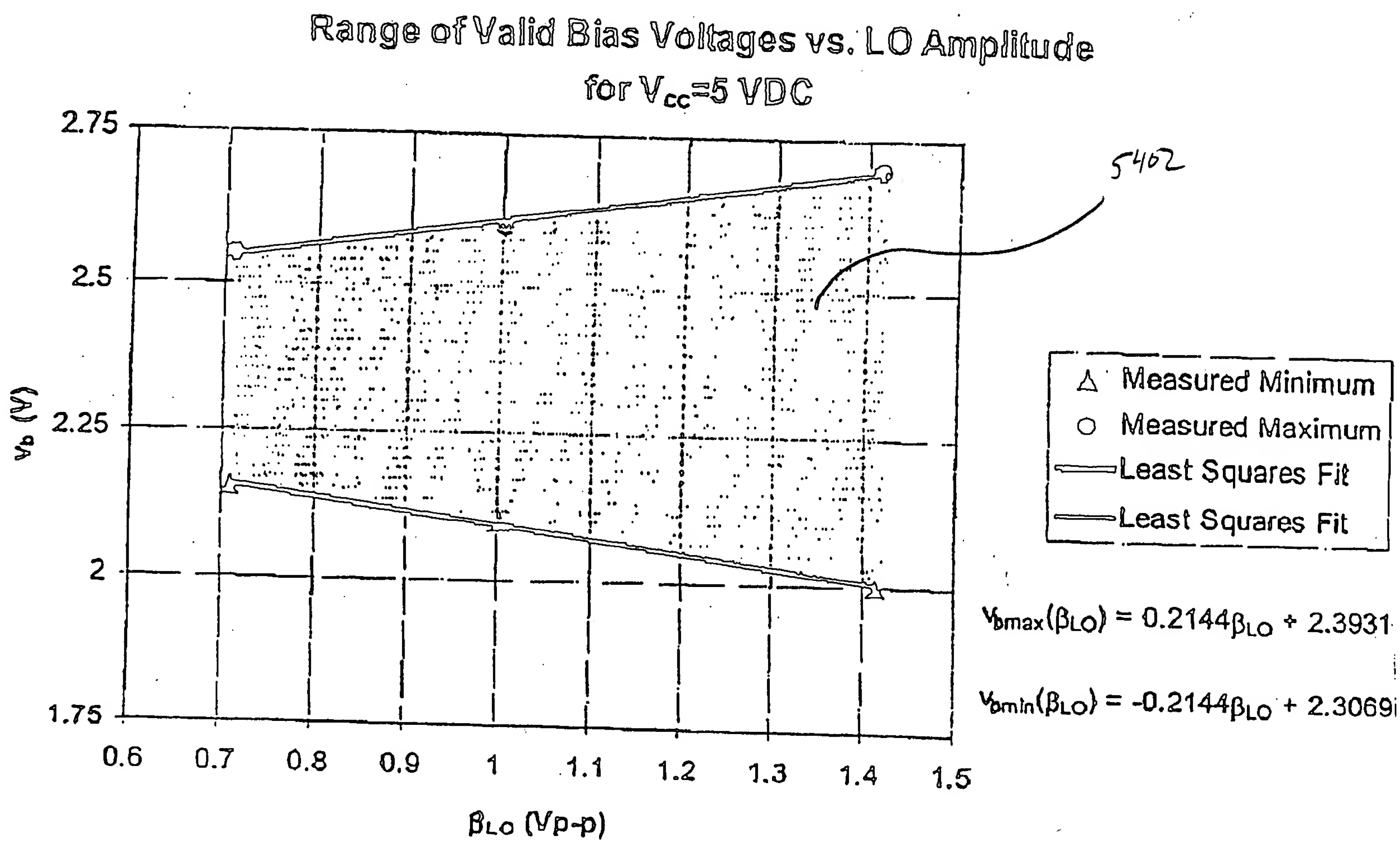
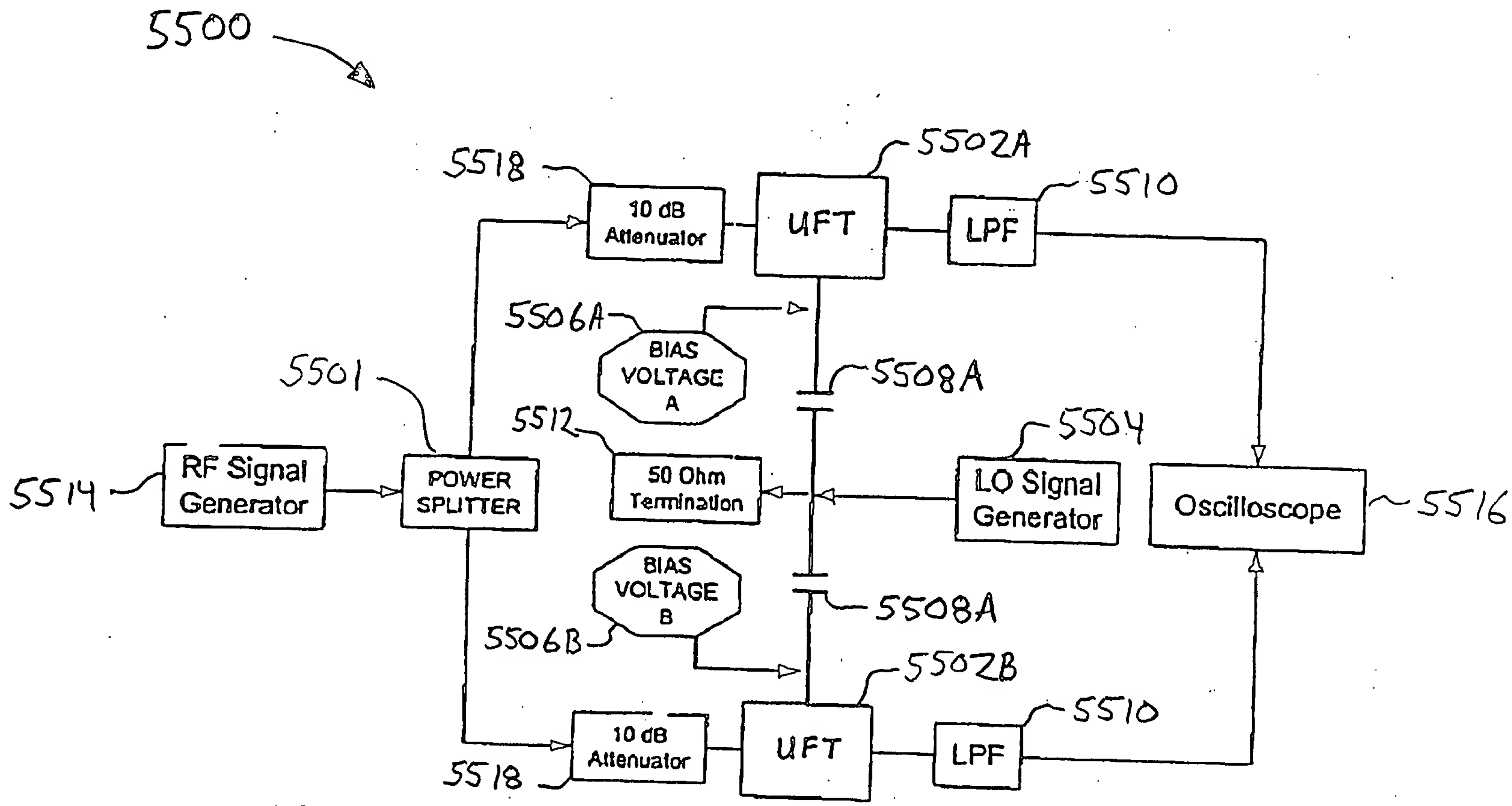
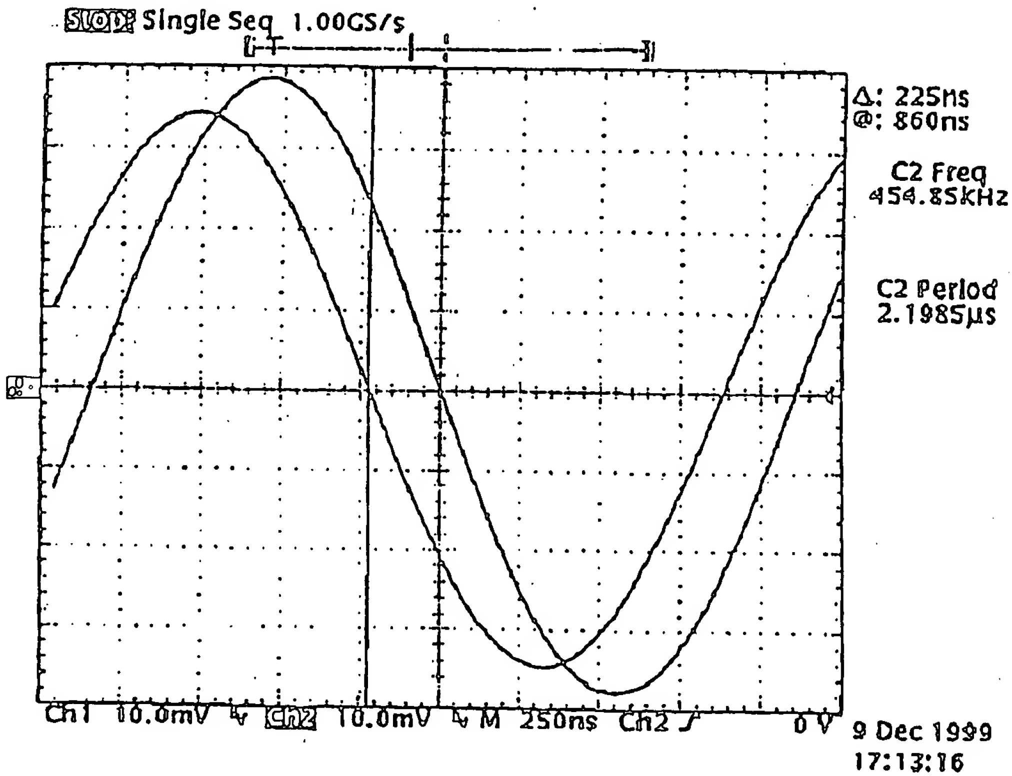

Range of Valid Bias Voltages vs. LO Amplitude
for V_{cc}=5 VDC
2.75
2.5
2.25
2
1.75
v_b (V)
0.6
0.7
0.8
0.9
1
1.1
1.2
1.3
1.4
1.5
β_{LO} (Vp-p)
5402
Measured Minimum
Measured Maximum
Least Squares Fit
Least Squares Fit
$V_{bmax}(\beta_{LO}) = 0.2144\beta_{LO} + 2.3931$
$V_{bmin}(\beta_{LO}) = -0.2144\beta_{LO} + 2.3069$

FIG. 54



A block diagram of a circuit where the phase of the two outputs can be adjusted independently by setting the LO bias voltages.

FIG. 55



Measured phase shift for the design example.

FIG. 56

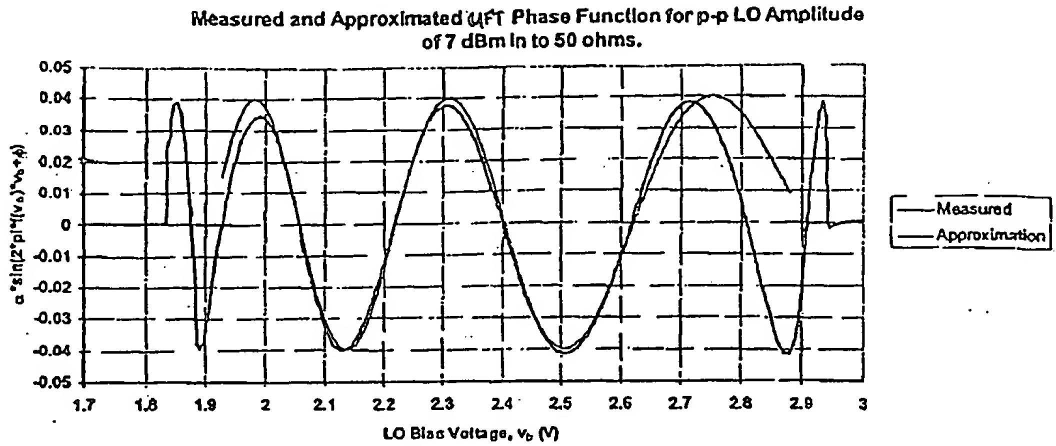


FIG. 57A

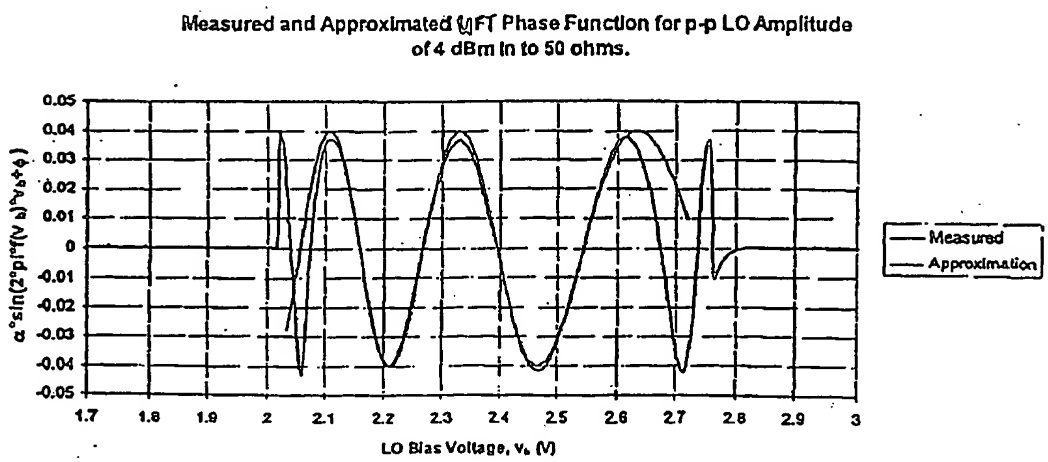


FIG. 57B

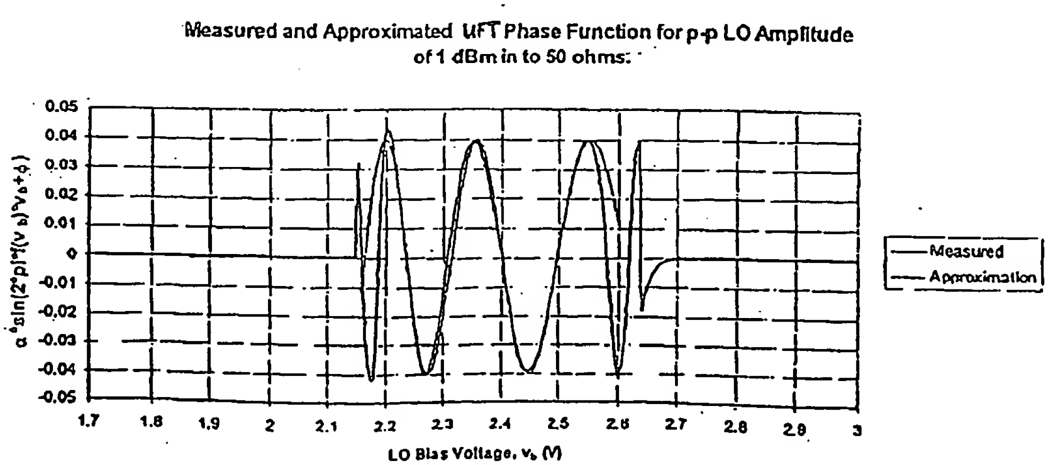


FIG. 57C

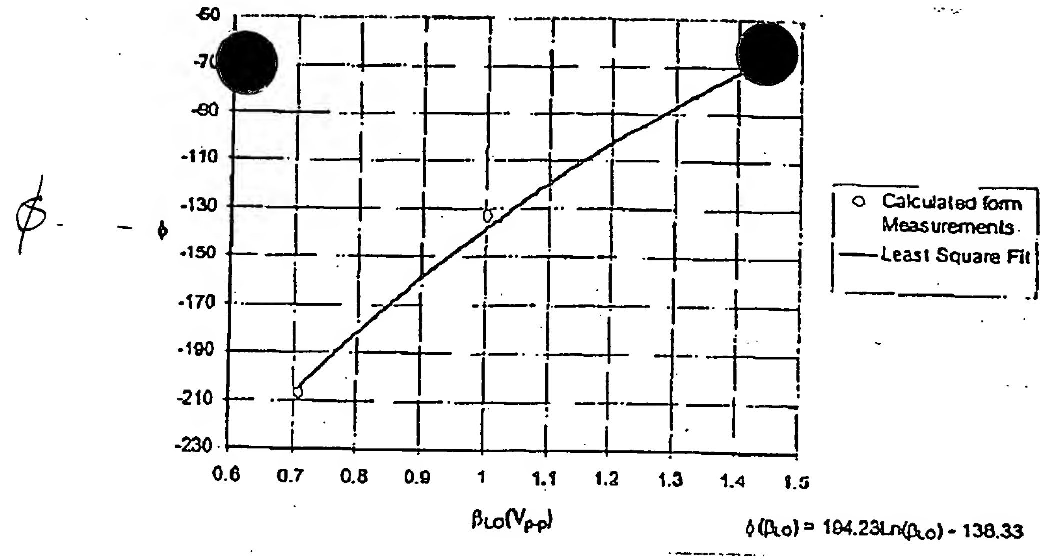


FIG. 58A

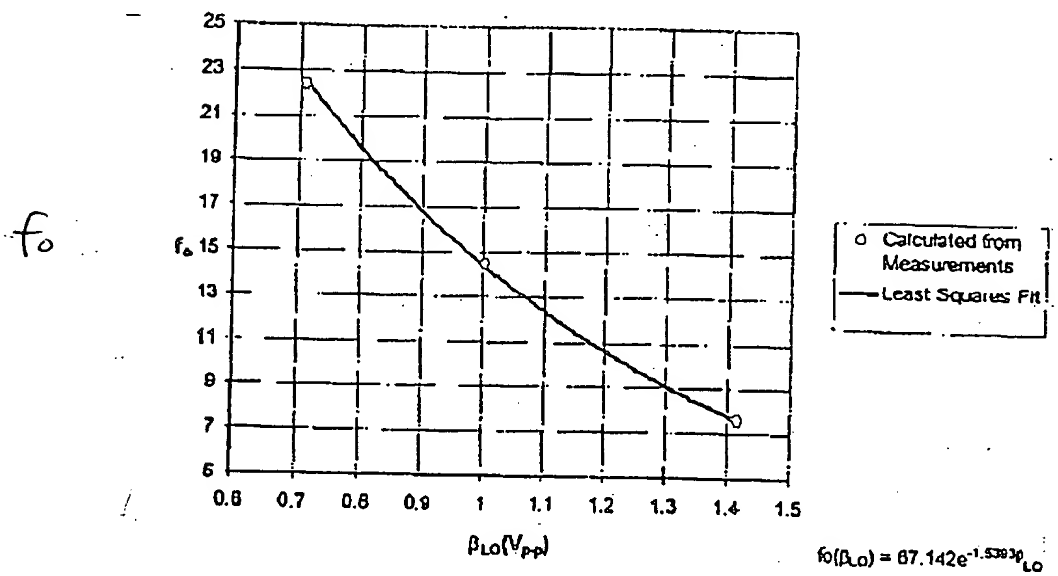


FIG. 58B

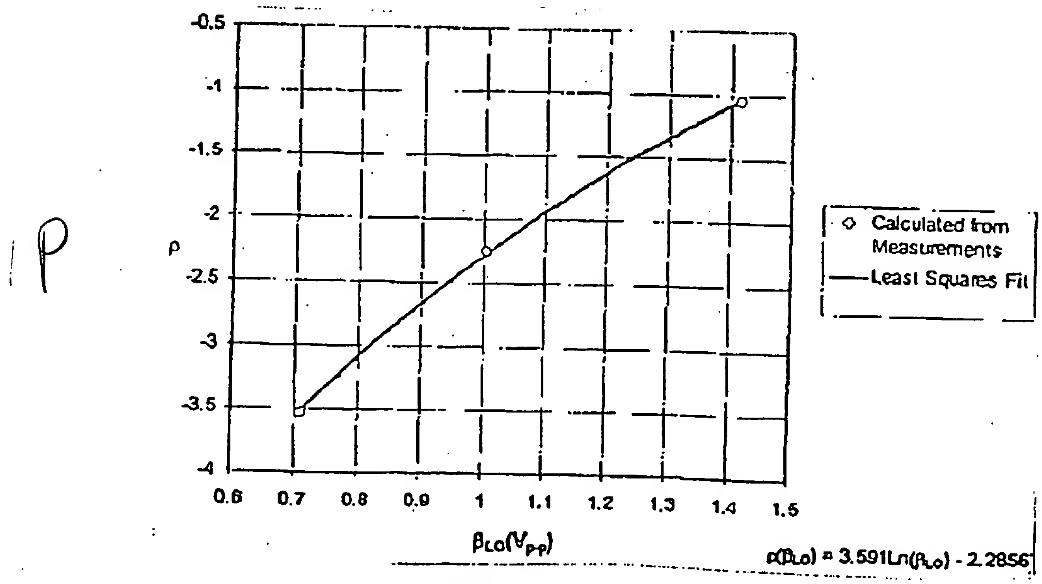


FIG. 58C

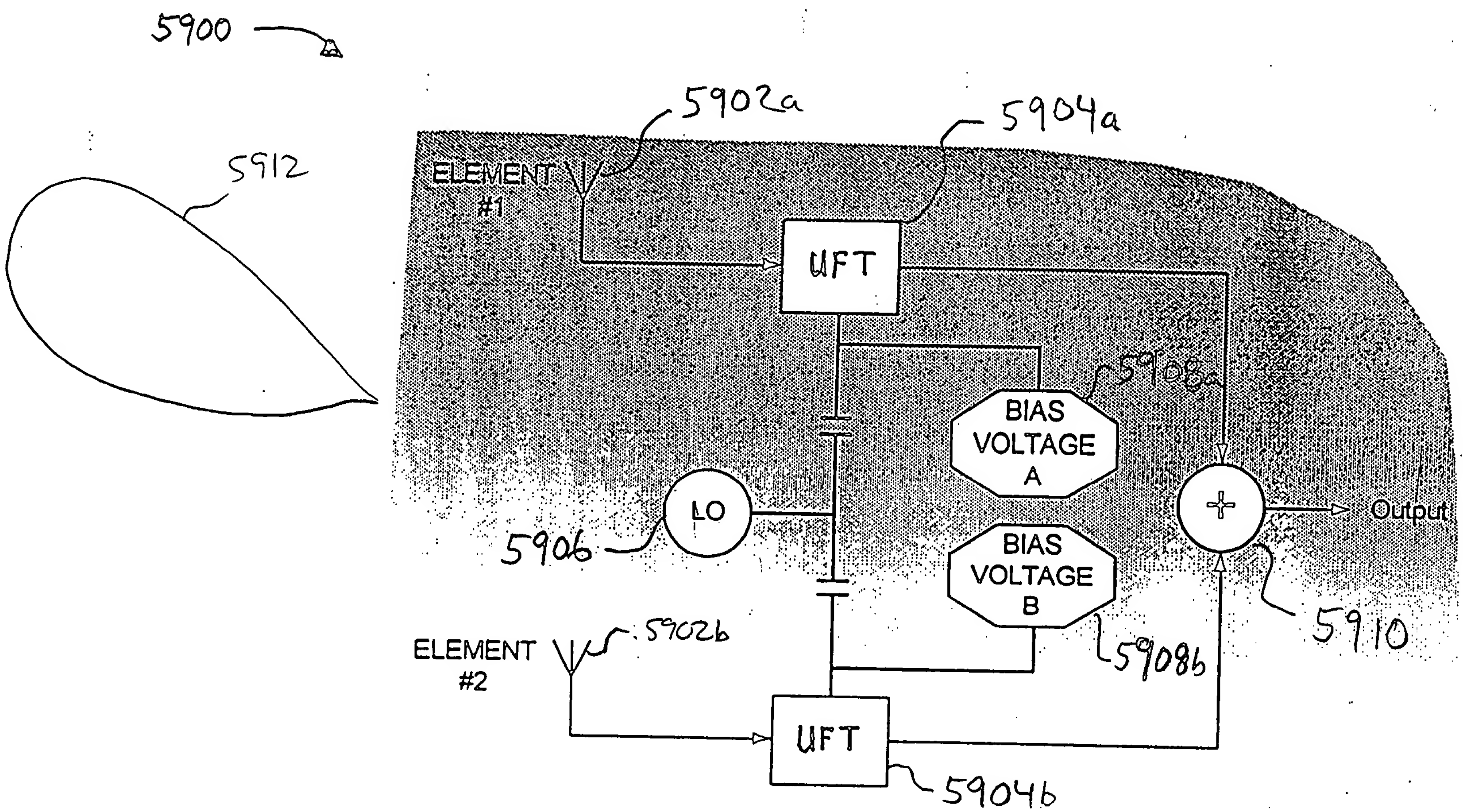

5900
5912
5902a
5904a
ELEMENT #1
UFT
5908a
BIAS VOLTAGE A
LO
5906
+
Output
BIAS VOLTAGE B
5910
ELEMENT #2
5902b
5908b
UFT
5904b

FIG. 59

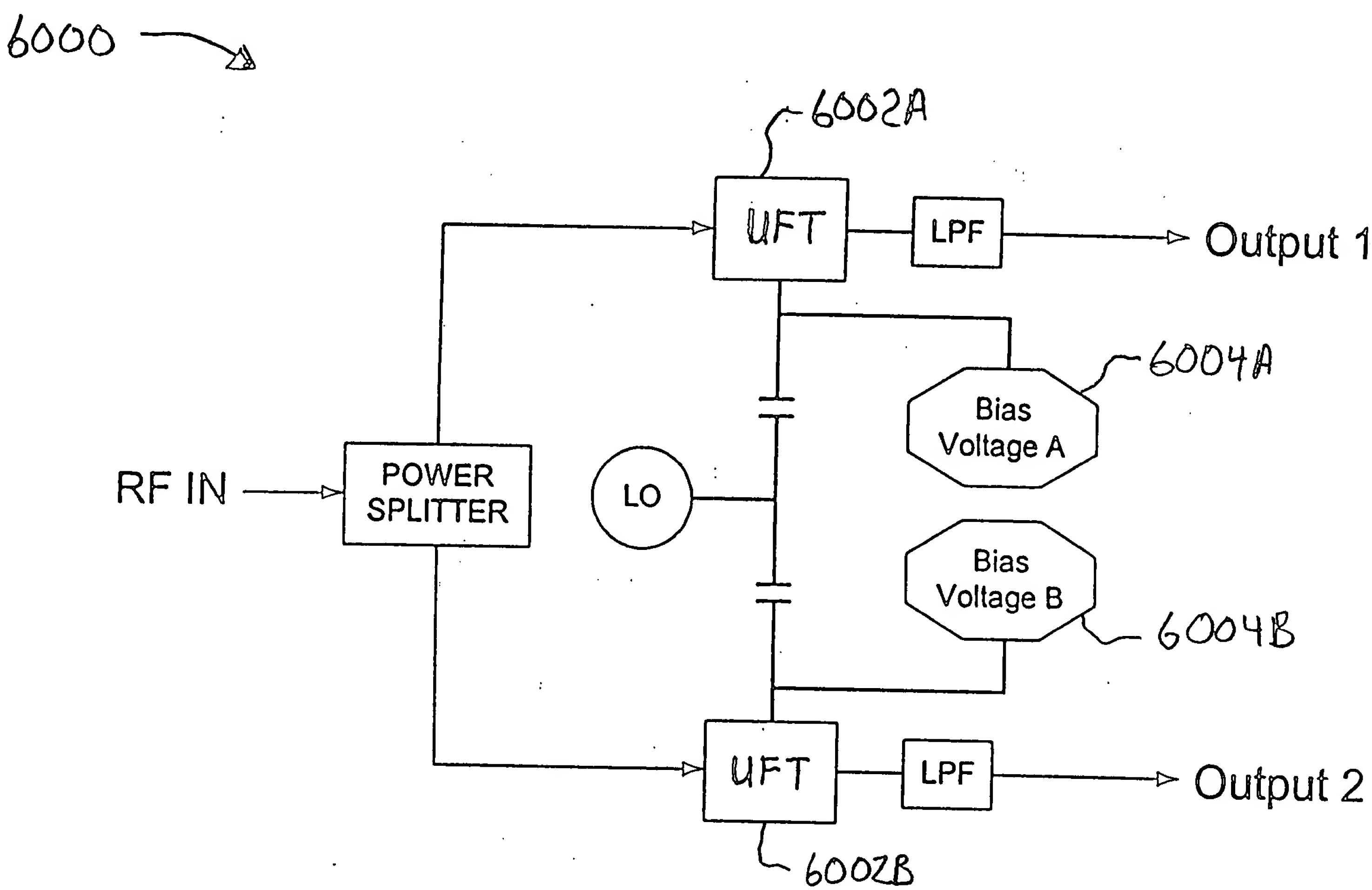

6000
6002A
UFT
LPF
Output 1
6004A
Bias
Voltage A
RF IN
POWER
SPLITTER
LO
Bias
Voltage B
6004B
UFT
LPF
Output 2
6002B

FIG. 60

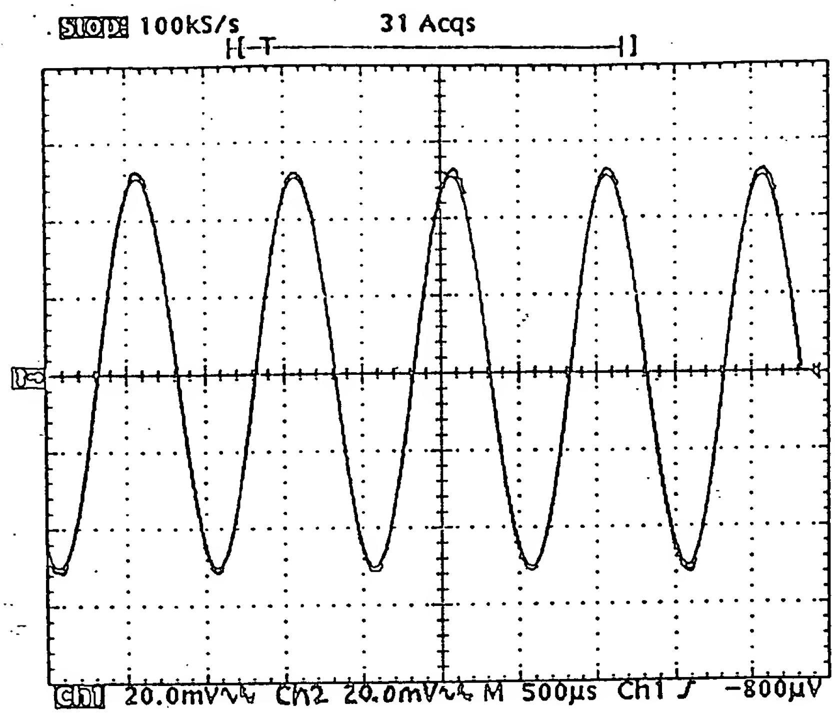


FIG. 61A

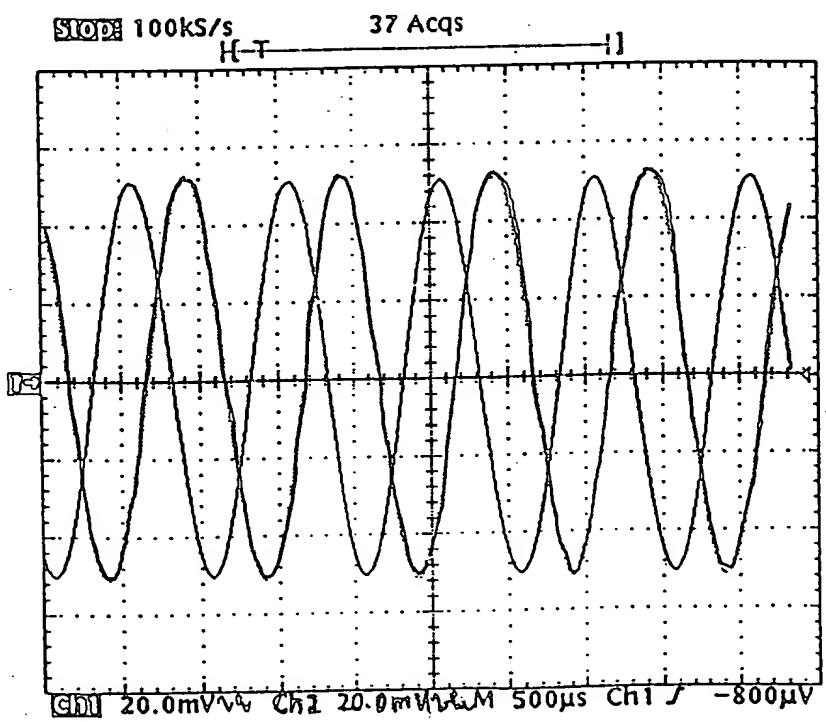


FIG. 61B

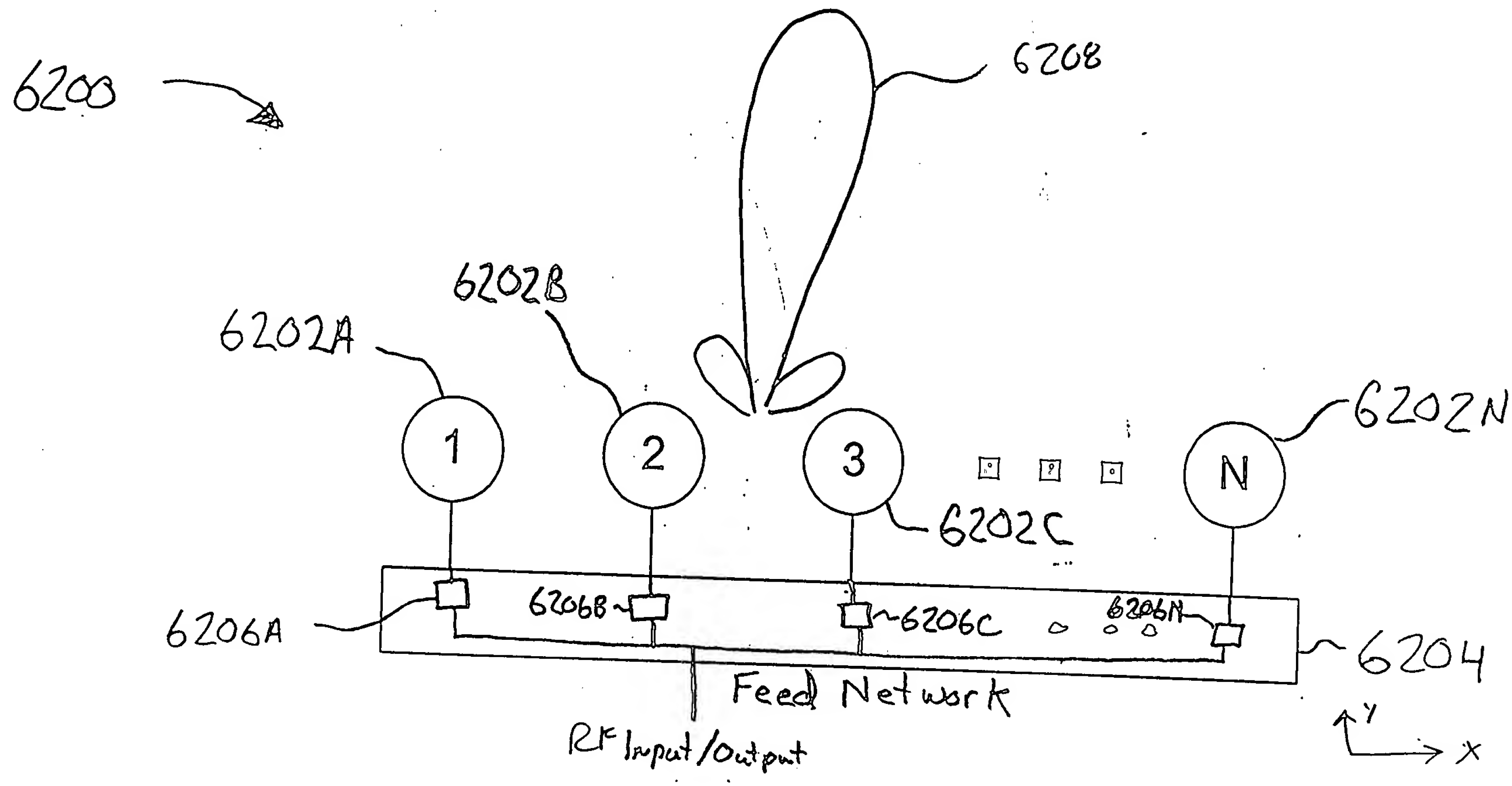

6200
6208
6202A
6202B
1
2
3
N
6202C
6202N
6206A
6206B
6206C
6206N
6204
Feed Network
RF Input/Output
Y
X

FIG. 62

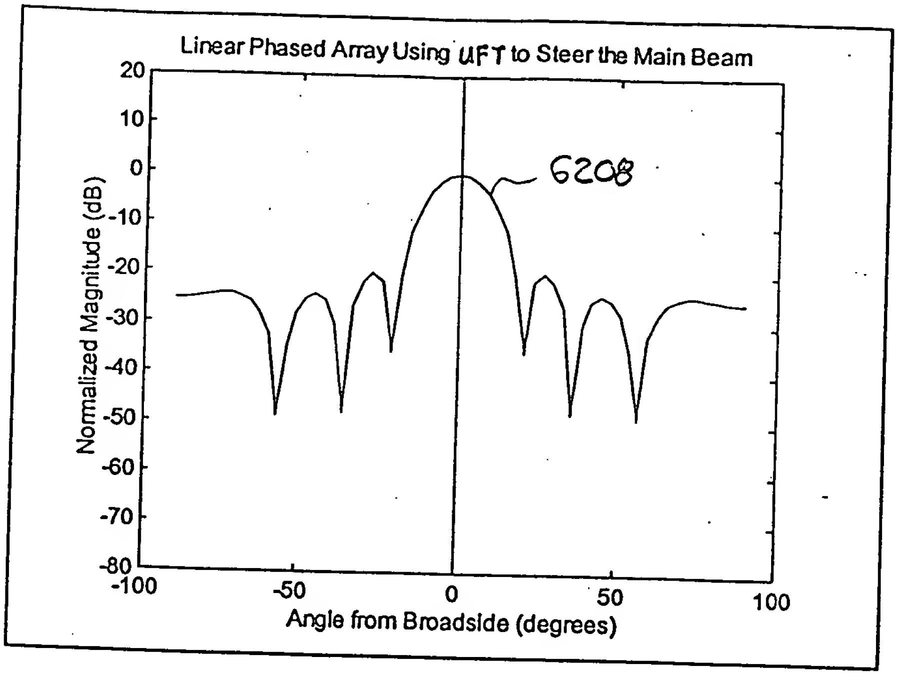


FIG. 63A

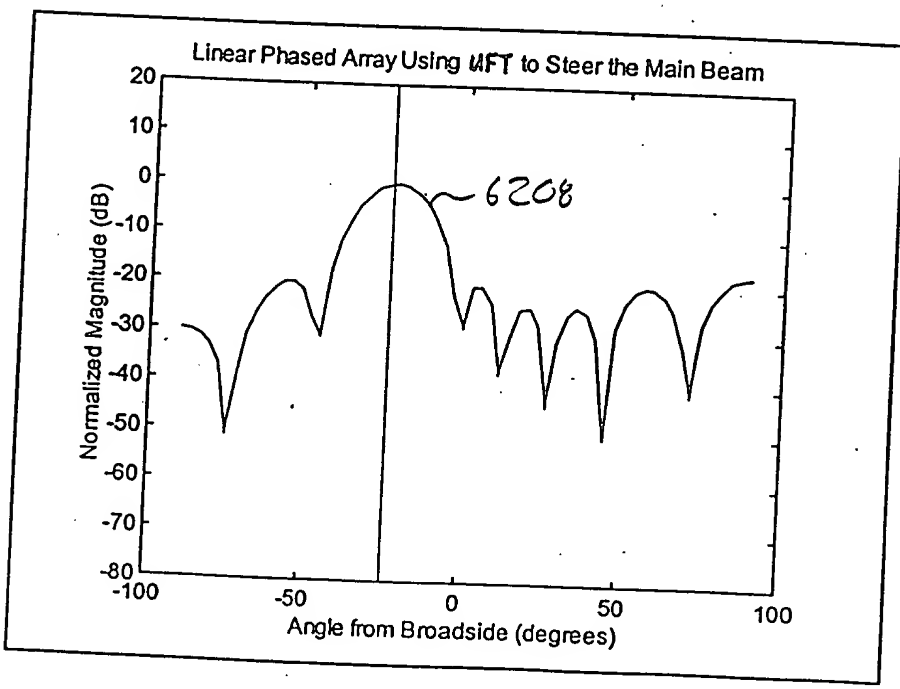


FIG. 63B

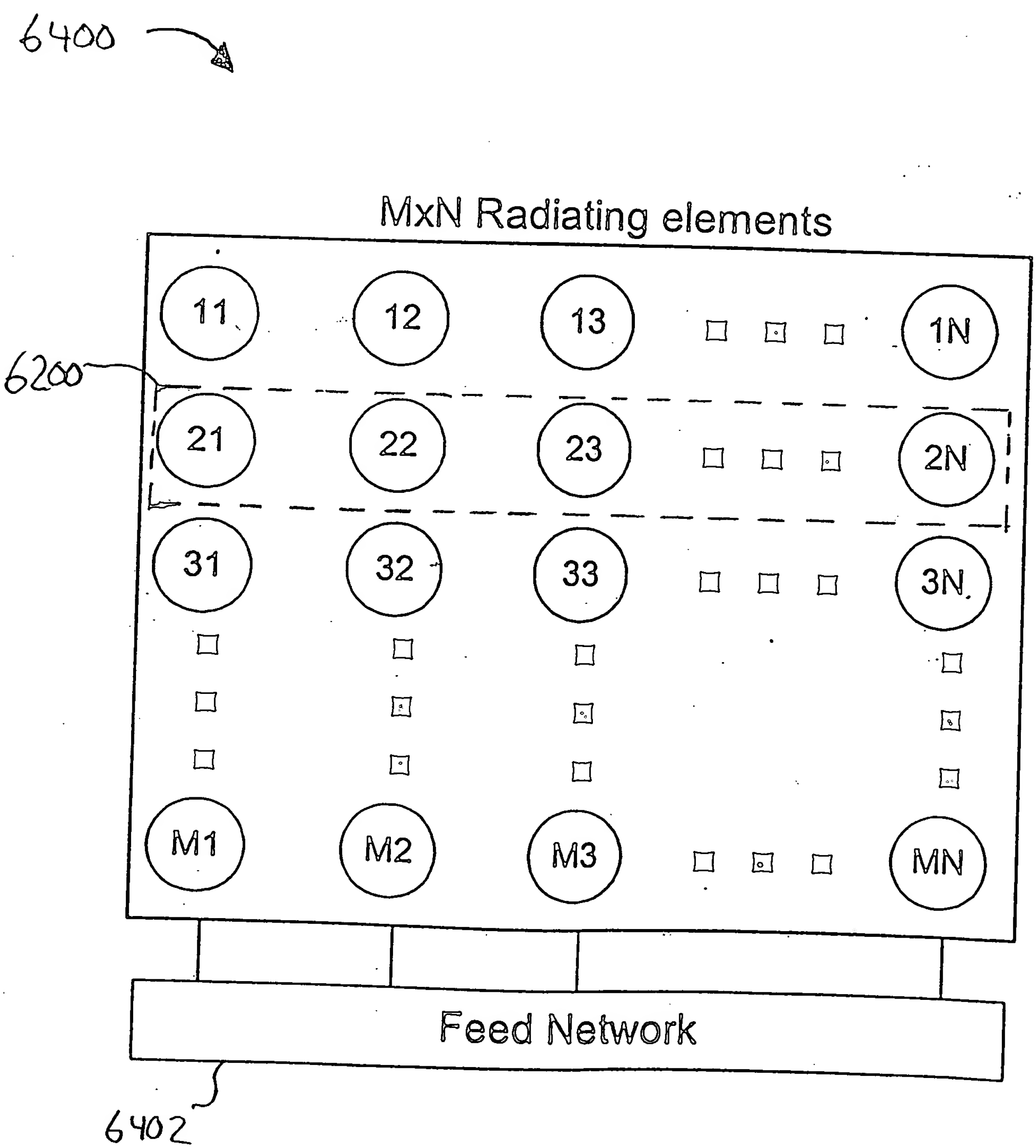

6400
MxN Radiating elements
11
12
13
1N
6200
21
22
23
2N
31
32
33
3N
M1
M2
M3
MN
Feed Network
6402

FIG 64

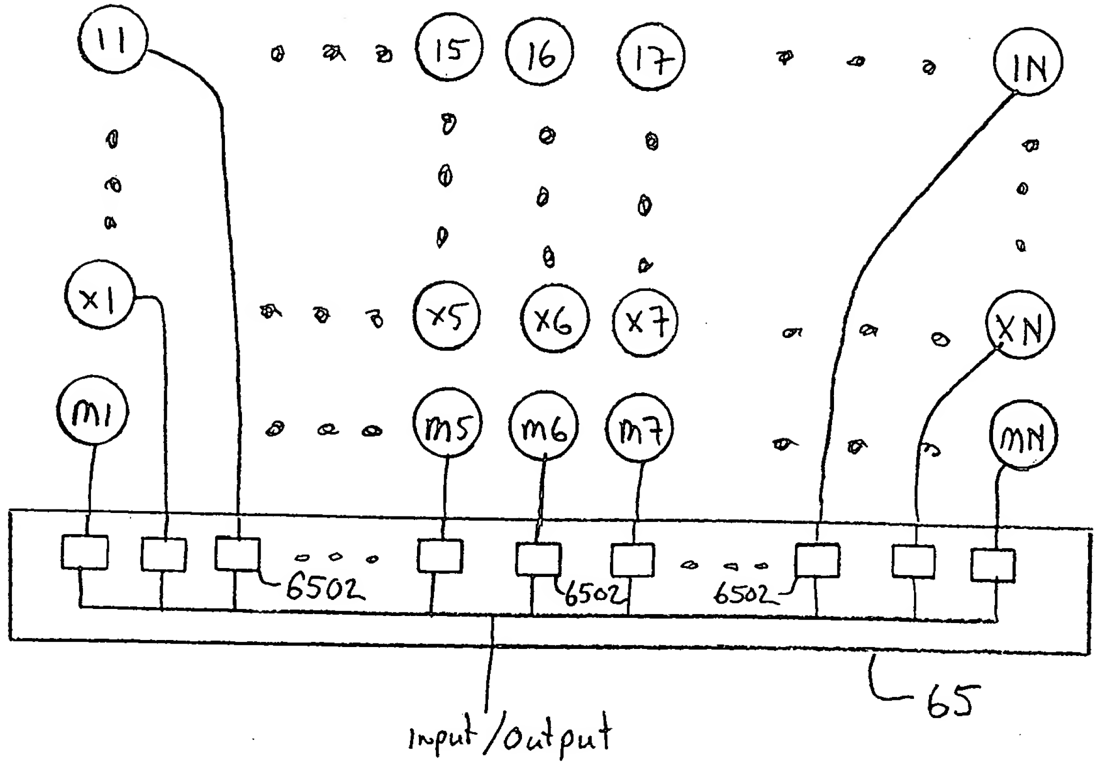


FIG. 65A

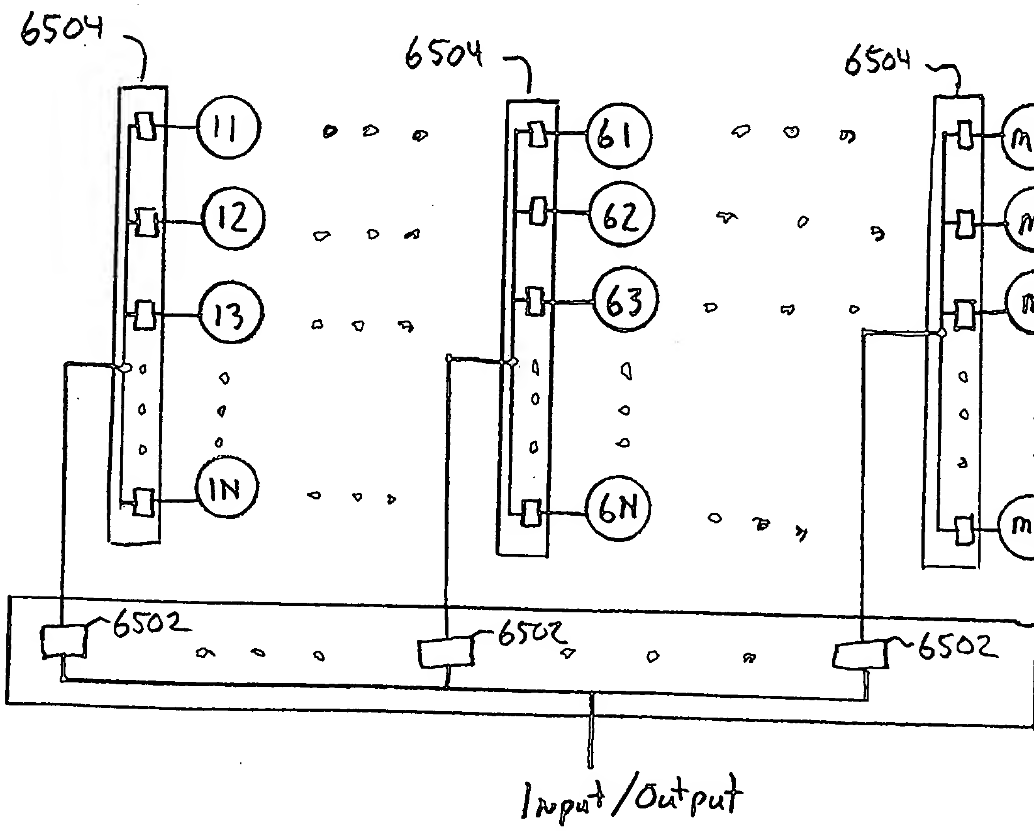


FIG. 65B

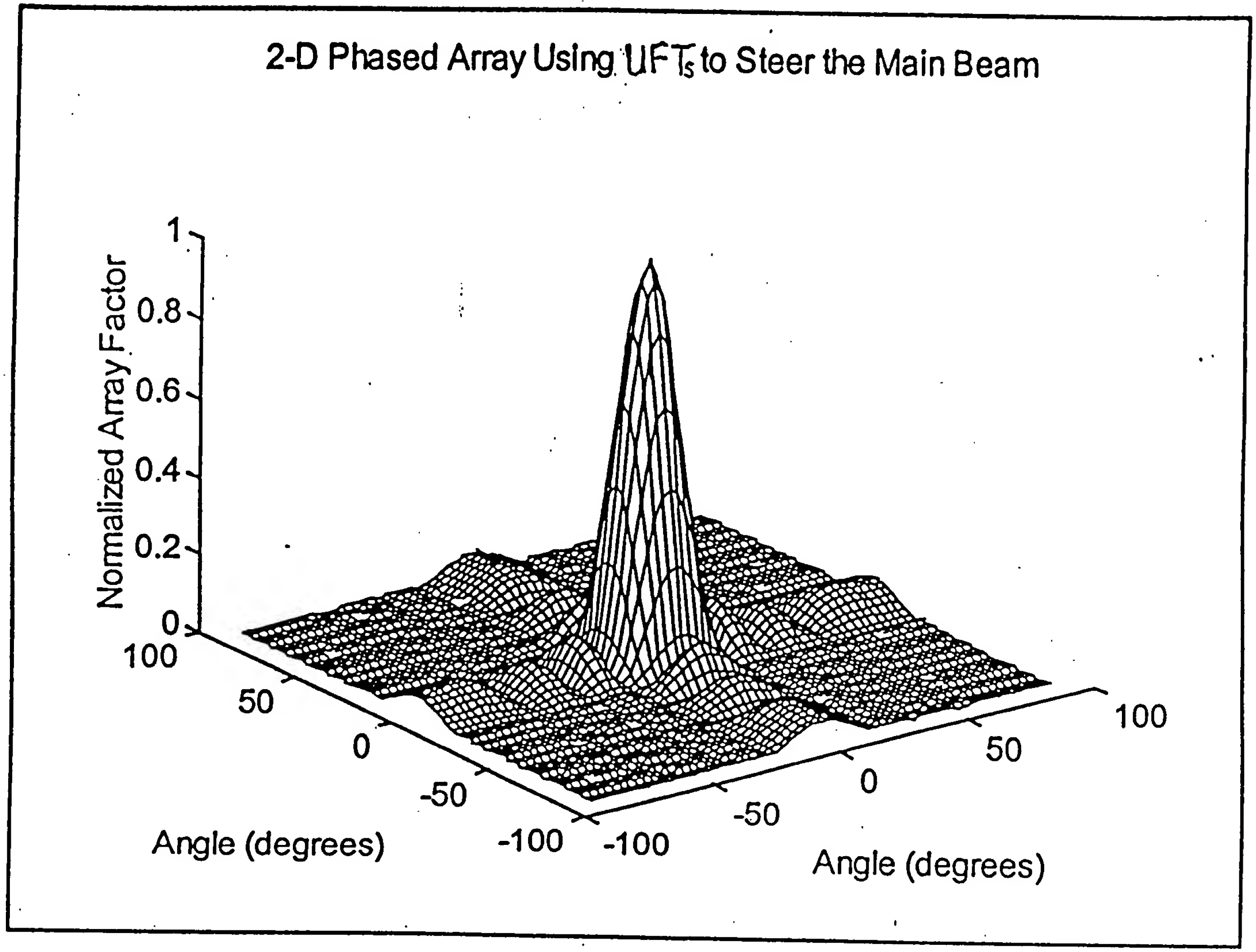

2-D Phased Array Using UFTs to Steer the Main Beam
Normalized Array Factor
1
0.8
0.6
0.4
0.2
0
100
50
0
-50
-100
Angle (degrees)
-100
-50
0
50
100
Angle (degrees)

FIG 66A

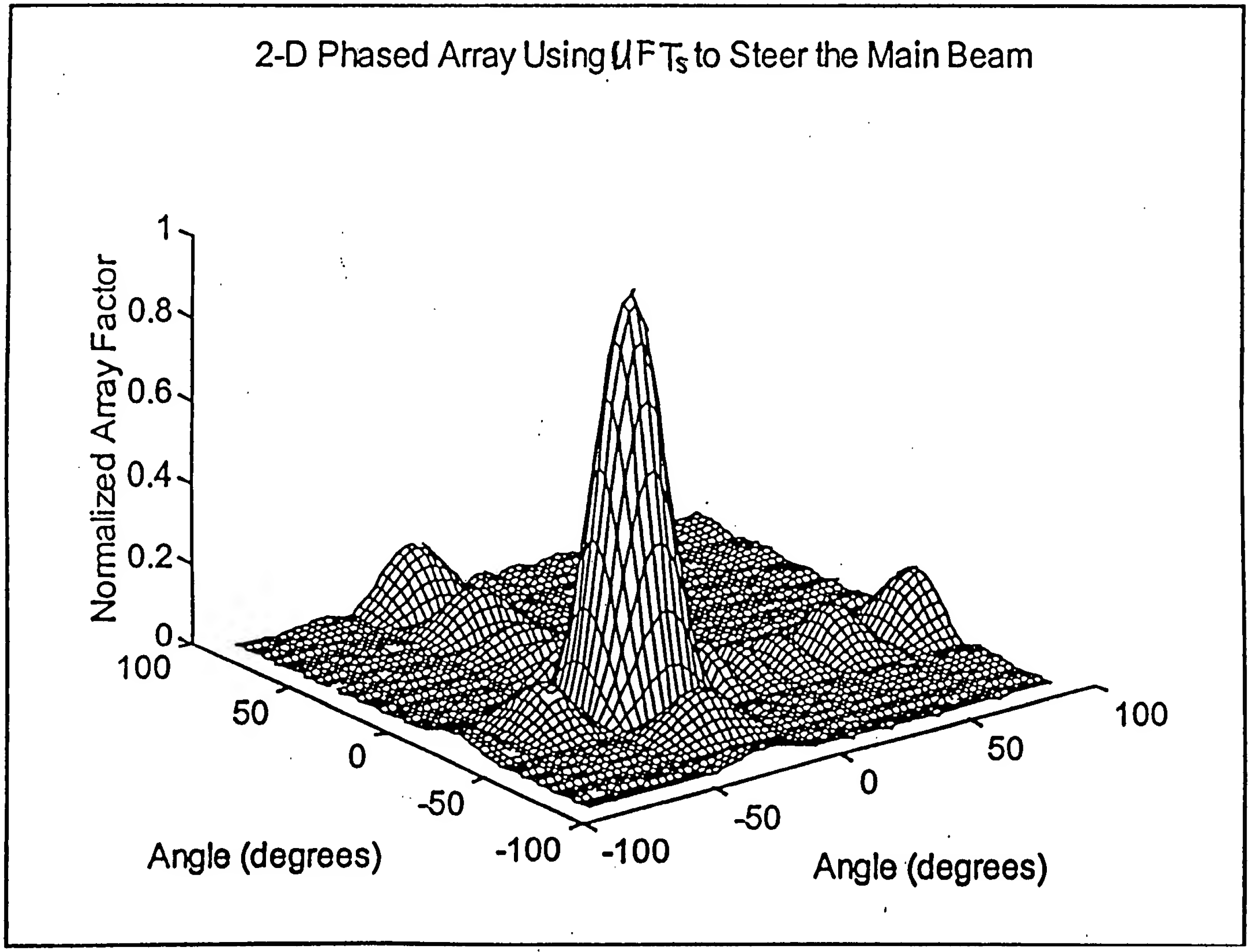

2-D Phased Array Using UFTs to Steer the Main Beam
Normalized Array Factor
1
0.8
0.6
0.4
0.2
0
100
50
0
-50
-100
Angle (degrees)
-100
-50
0
50
100
Angle (degrees)

FIG. 66B

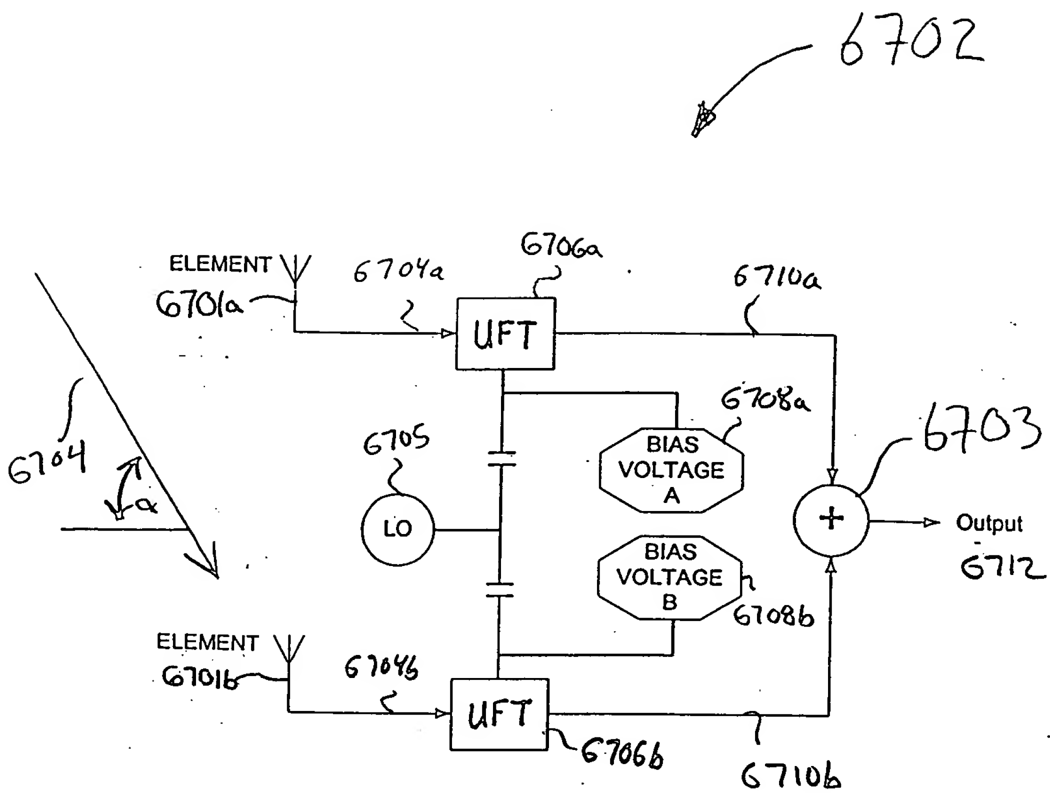


FIG. 67 A

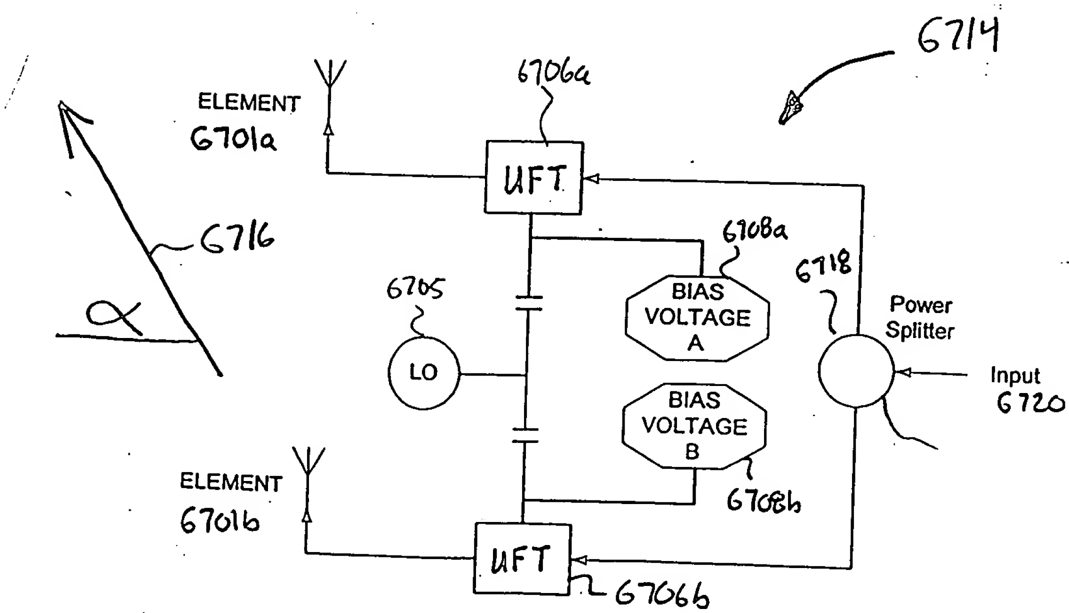
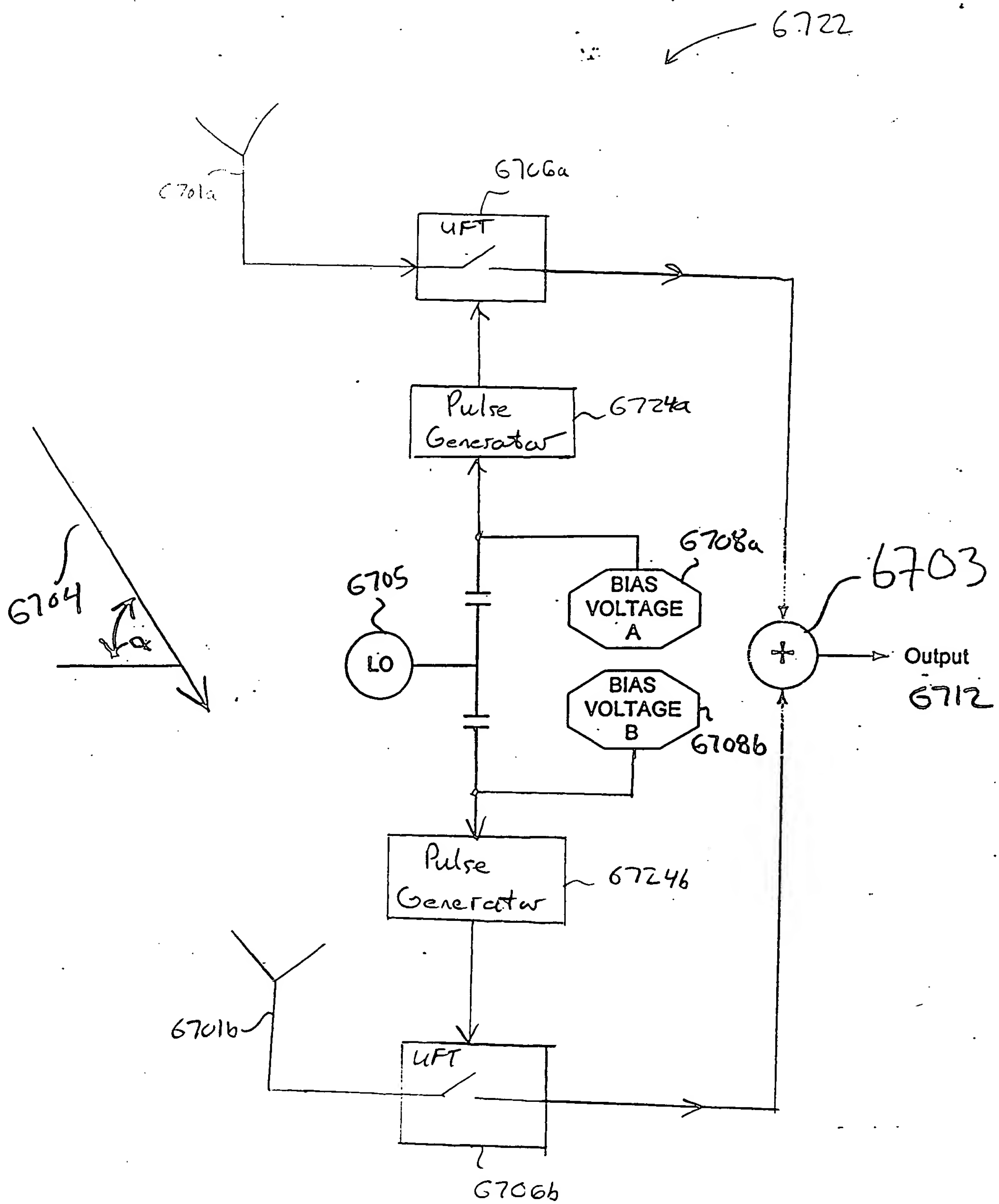
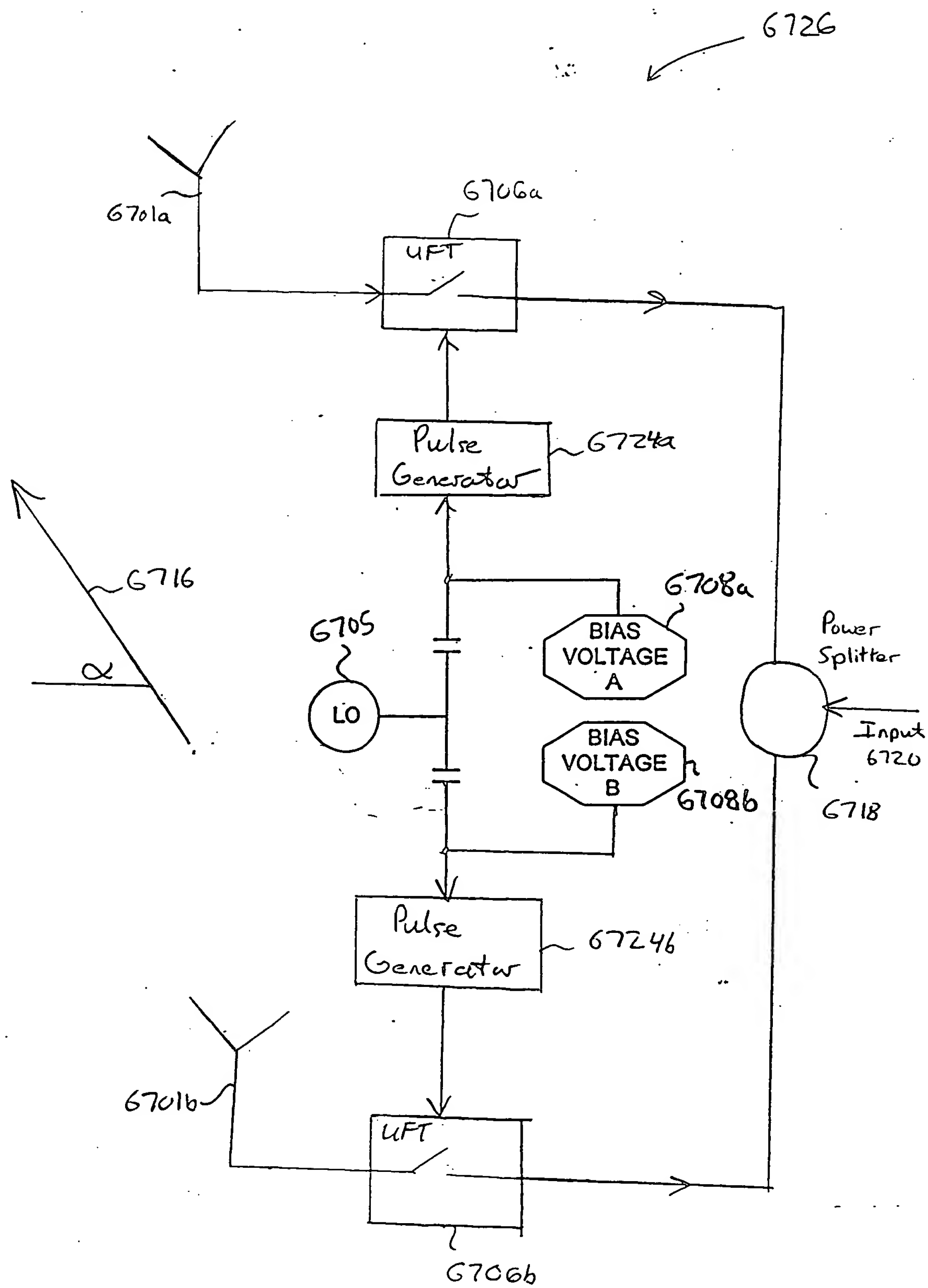


FIG. 67B



6722
6701a
6706a
UFT
Pulse Generator
6724a
6708a
6705
6703
6704
α
BIAS VOLTAGE A
LO
Output
6712
BIAS VOLTAGE B
6708b
Pulse Generator
6724b
6701b
UFT
6706b

FIG. 67C



6726
6701a
6706a
UFT
Pulse
Generator
6724a
6716
α
6708a
BIAS
VOLTAGE
A
6705
LO
BIAS
VOLTAGE
B
6708b
Power
Splitter
Input
6720
6718
Pulse
Generator
6724b
6701b
UFT
6706b

FIG. 67D

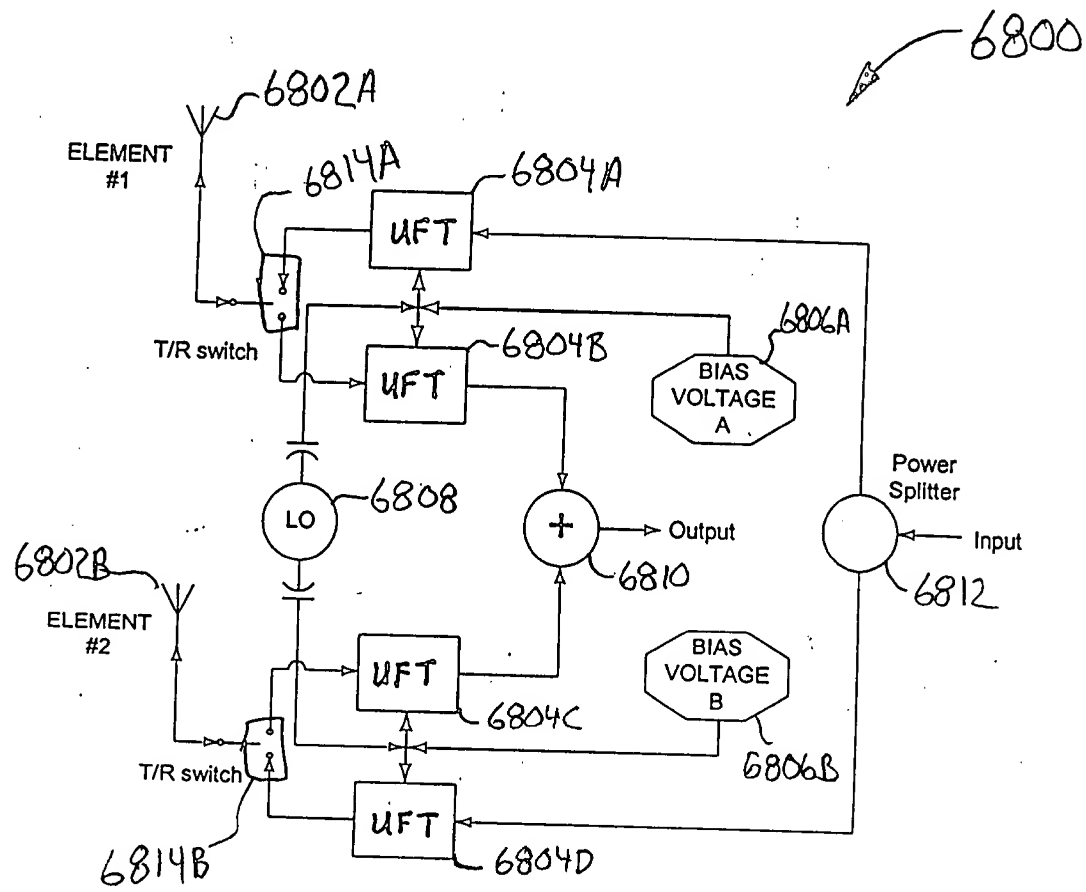

6800
6802A
ELEMENT
#1
6814A
6804A
UFT
T/R switch
6804B
UFT
6806A
BIAS
VOLTAGE
A
LO
6808
+
Output
6810
Power
Splitter
Input
6812
6802B
ELEMENT
#2
UFT
6804C
BIAS
VOLTAGE
B
T/R switch
6806B
UFT
6814B
6804D

FIG. 68A

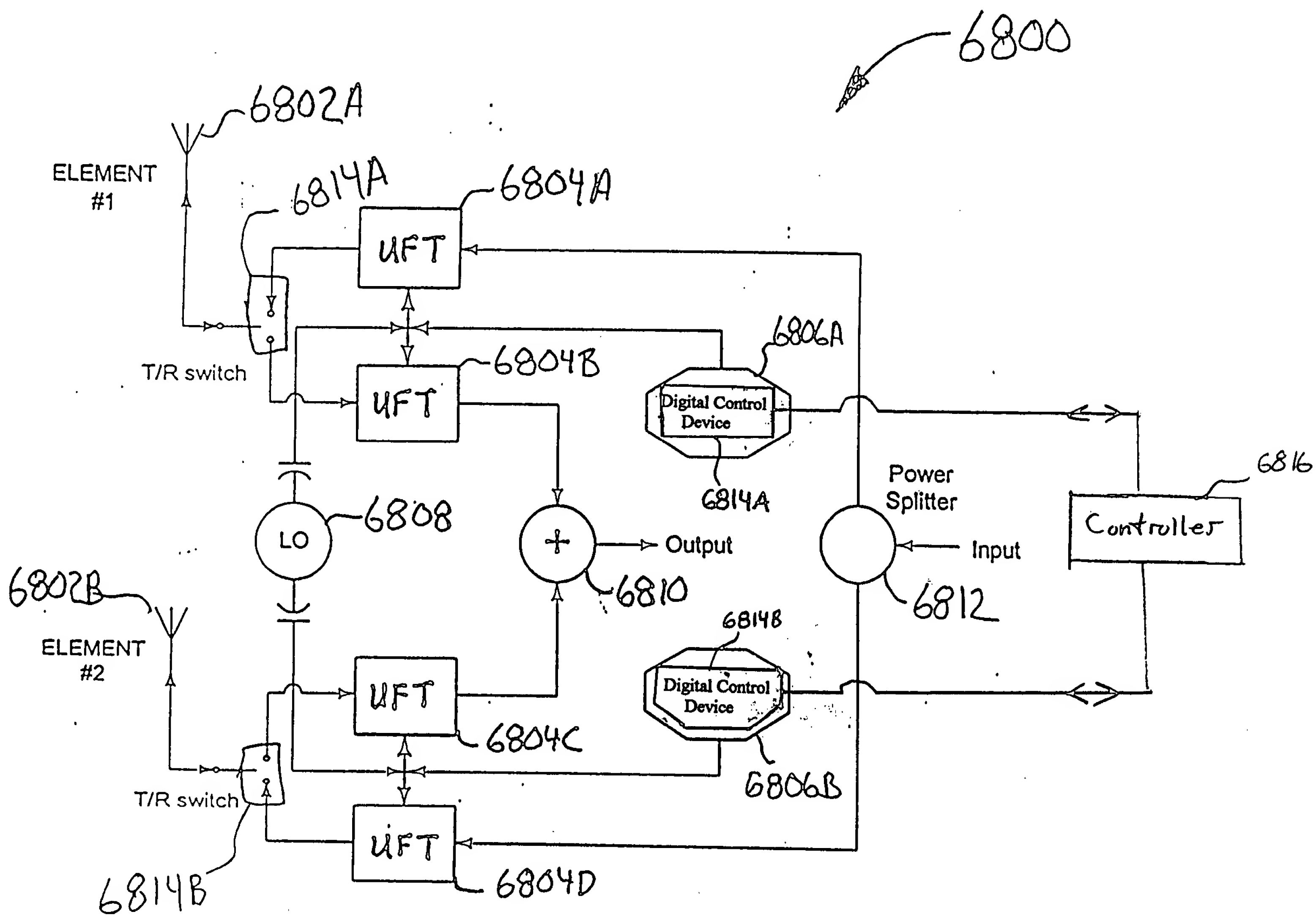

6800
6802A
ELEMENT #1
6814A
6804A
UFT
T/R switch
6804B
UFT
6806A
Digital Control Device
6814A
6808
LO
Output
6810
Power Splitter
Input
6812
6816
Controller
6802B
ELEMENT #2
6814B
Digital Control Device
UFT
6804C
6806B
T/R switch
6814B
UFT
6804D

FIG. 68B

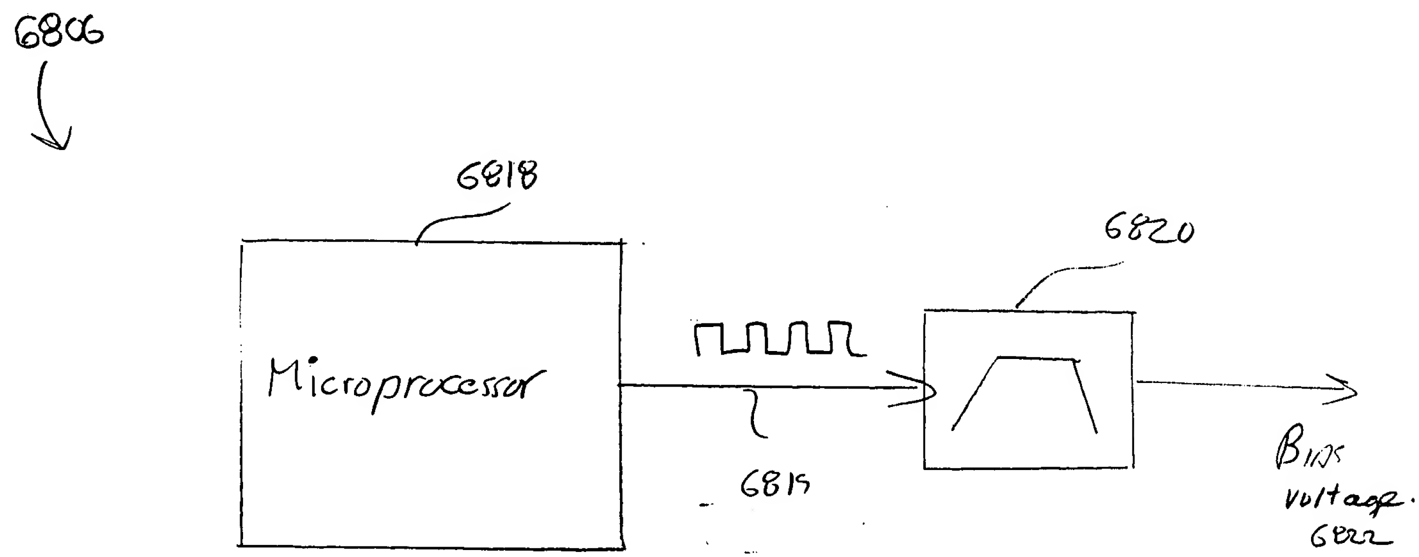


FIG. 68C

Radiation Pattern for a UFT Based, Two Element Phased Array
15 Degree Main Beam Angle, -20 Degree Null

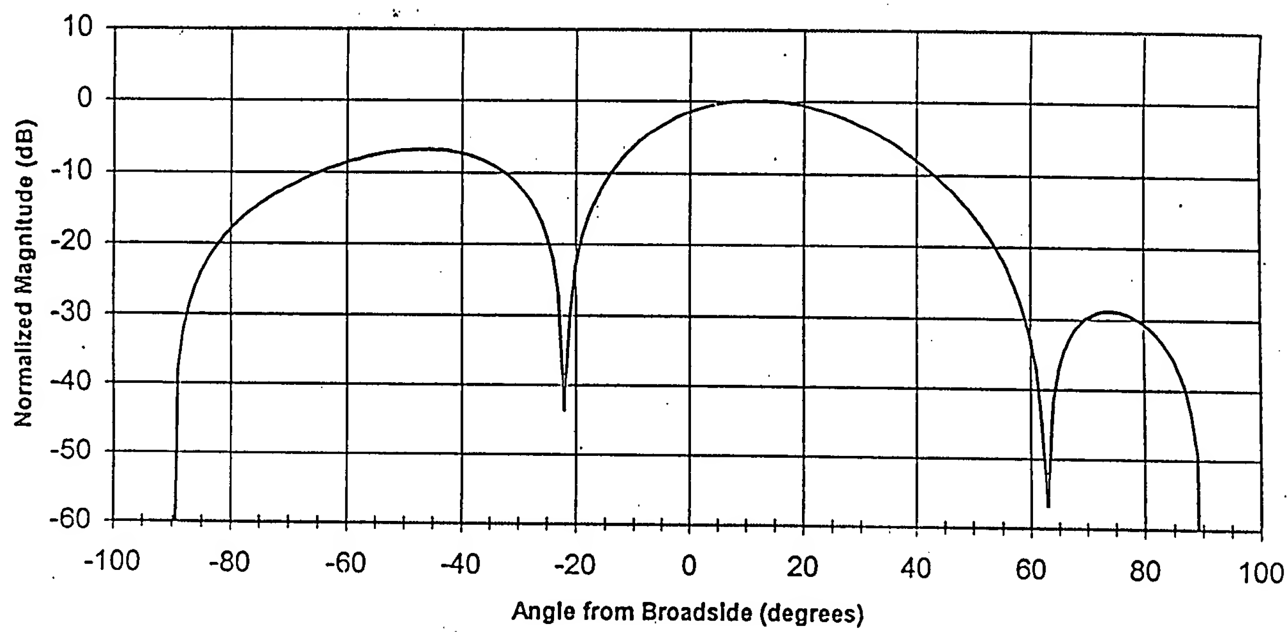


FIG. 69

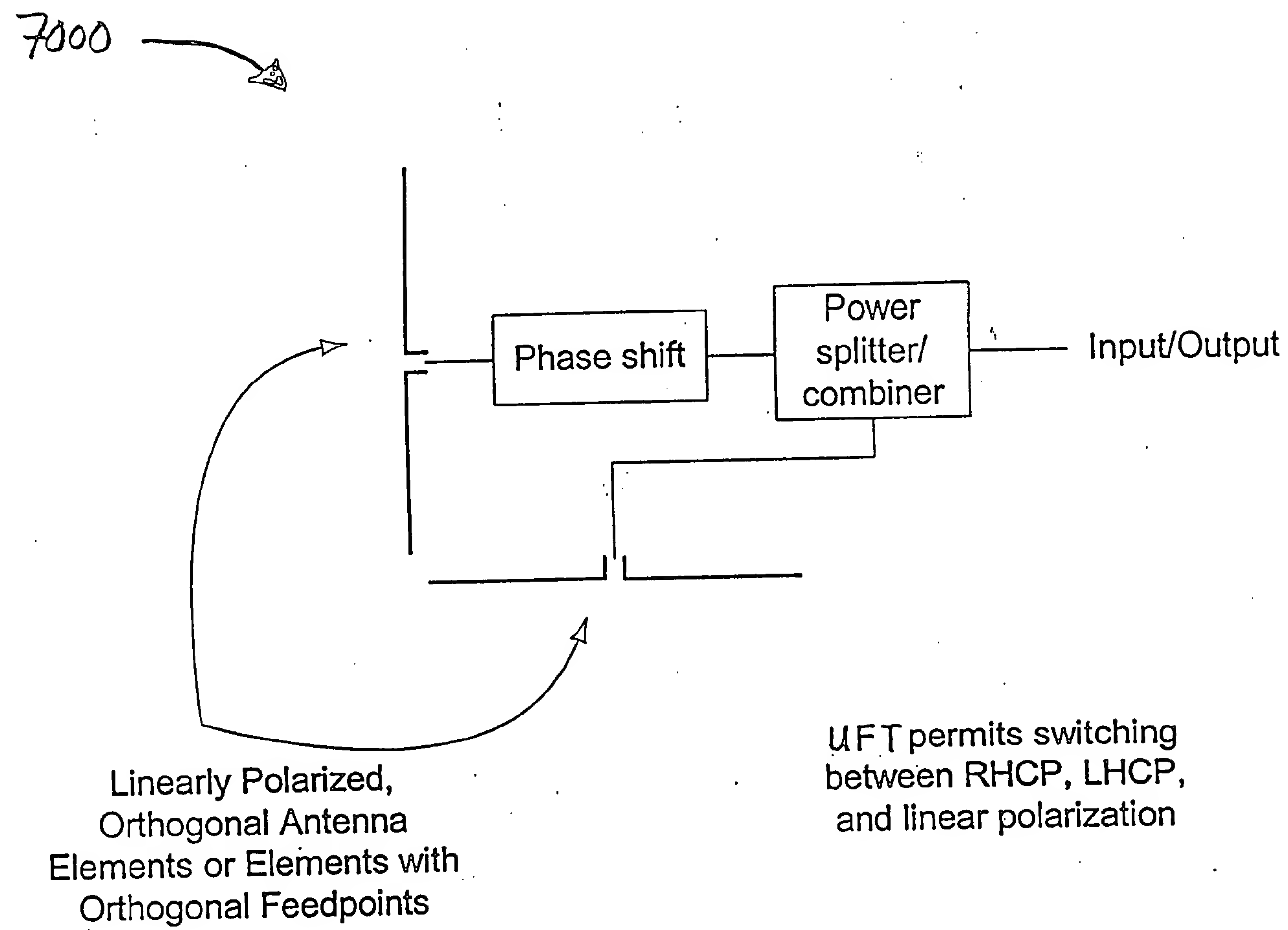

7000
Phase shift
Power splitter/ combiner
Input/Output
Linearly Polarized, Orthogonal Antenna Elements or Elements with Orthogonal Feedpoints
UFT permits switching between RHCP, LHCP, and linear polarization

FIG. 70

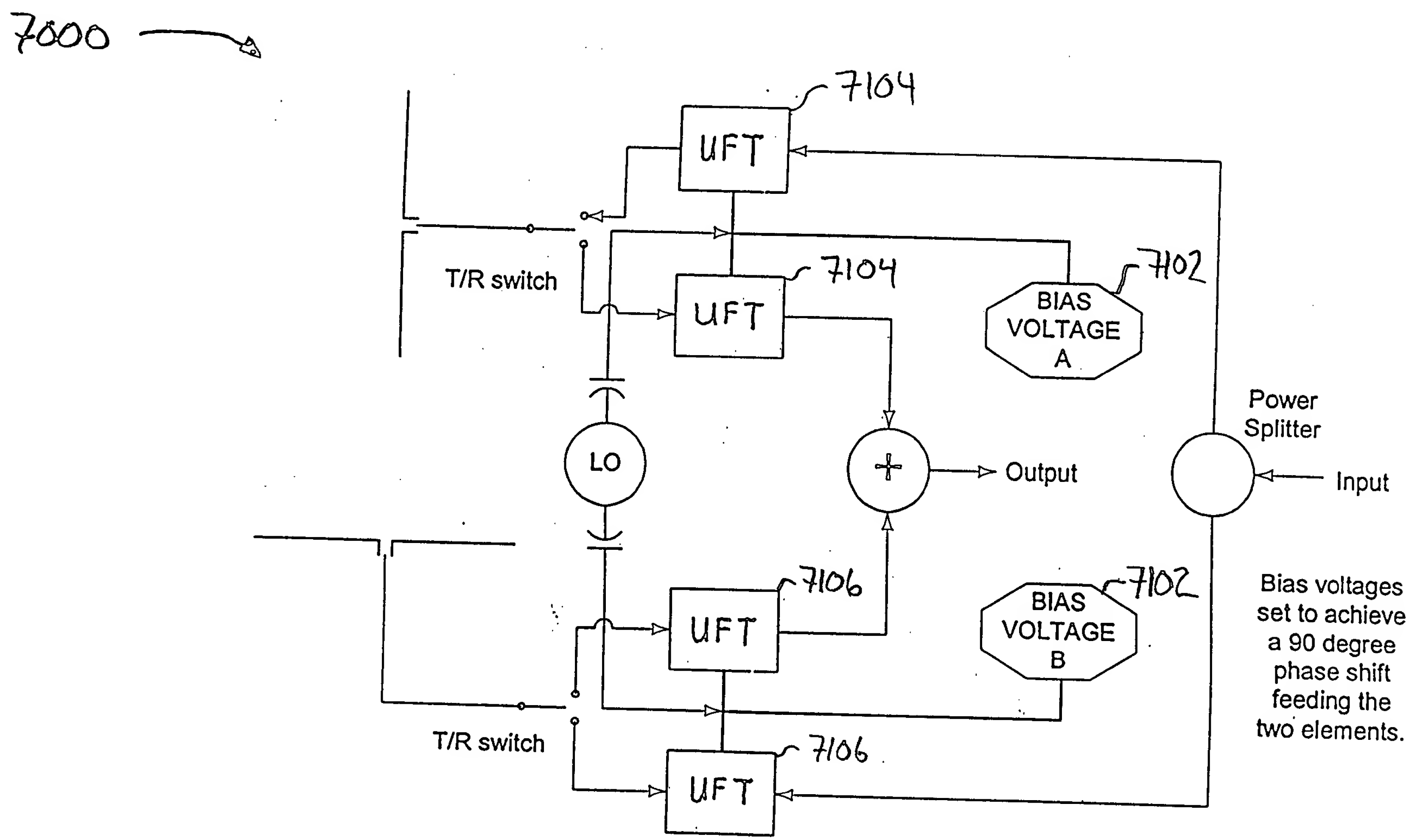
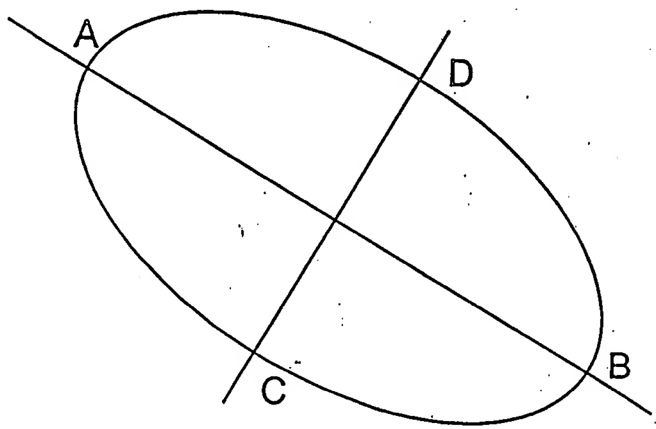

7000
7104
UFT
7104
UFT
T/R switch
BIAS
VOLTAGE
A
7102
LO
Output
Power
Splitter
Input
7106
UFT
BIAS
VOLTAGE
B
7102
T/R switch
7106
UFT
Bias voltages
set to achieve
a 90 degree
phase shift
feeding the
two elements.

FIG. 71



Ellipse representing an ellipticallypolarized wave

The axial ratio is the ratio of the length of the line segment AB to the length of the line segment CD

$$\text{Axial Ratio}=\frac{AB}{CD}$$

When AB=CD then the ideal axial ratio is achieved and pure circular polarization is realized

FIG. 72

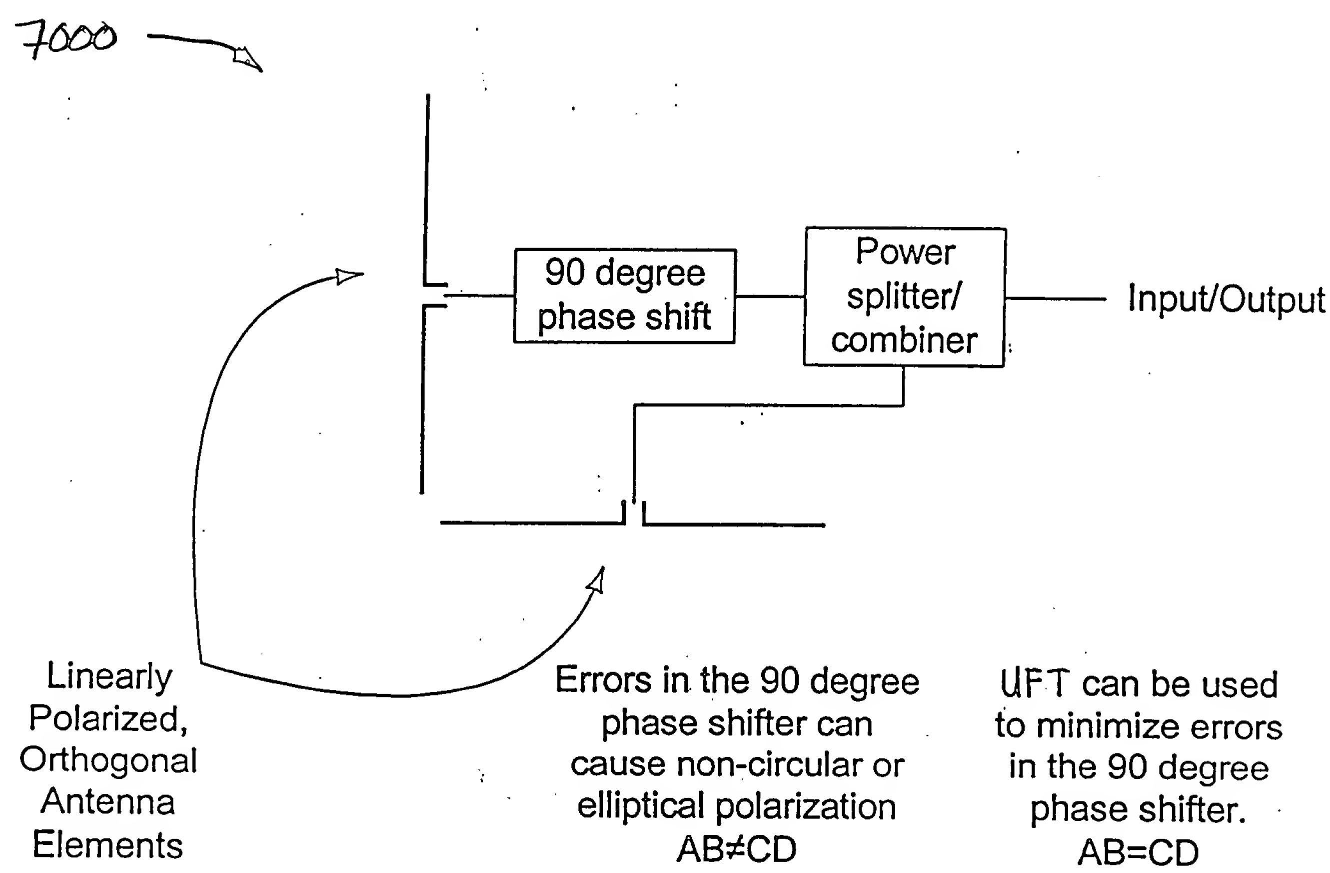

7000
90 degree phase shift
Power splitter/ combiner
Input/Output
Linearly Polarized, Orthogonal Antenna Elements
Errors in the 90 degree phase shifter can cause non-circular or elliptical polarization AB≠CD
UFT can be used to minimize errors in the 90 degree phase shifter. AB=CD

FIG. 73

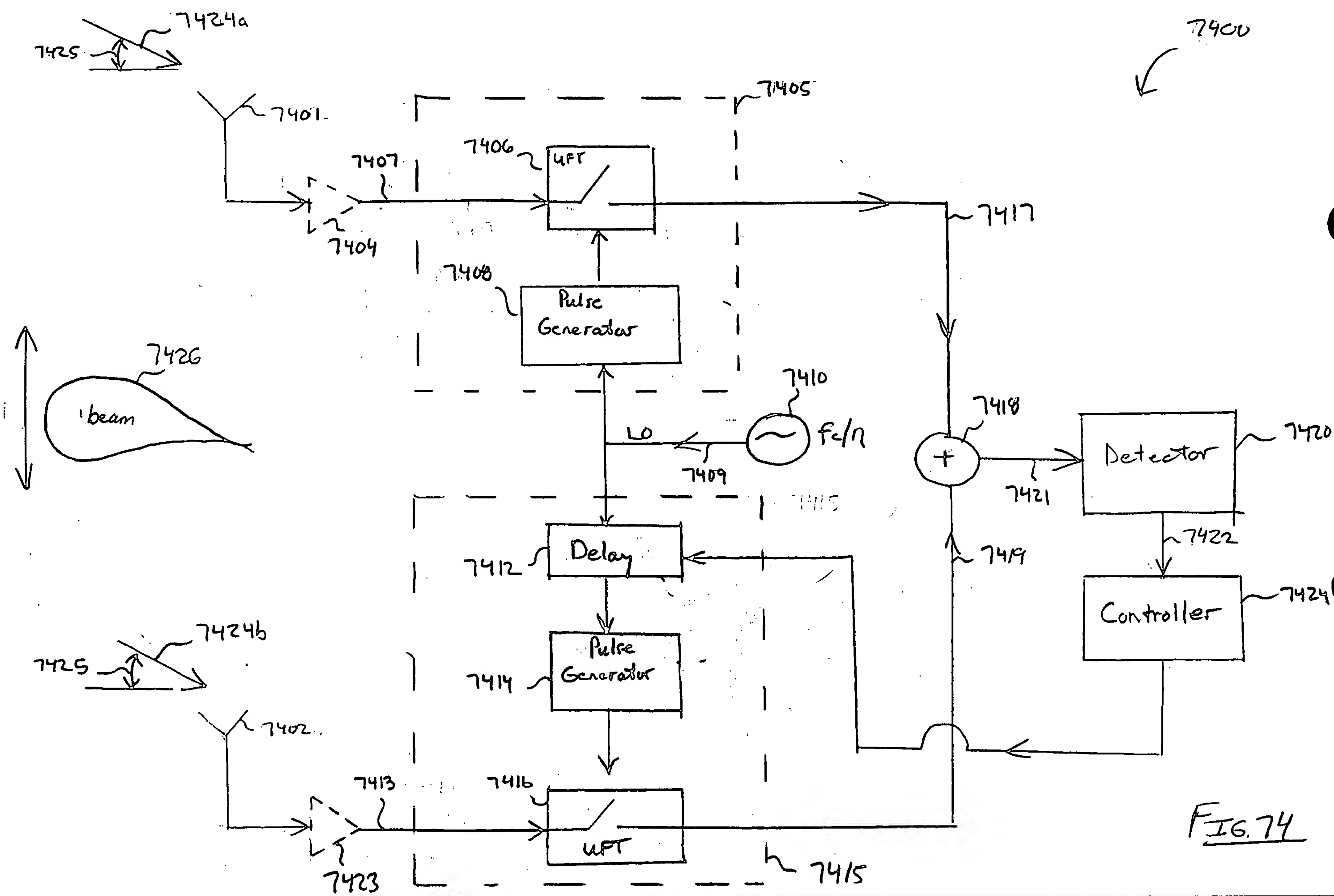

7400
7424a
7425
7401
7405
7406
UFT
7407
7404
7417
7408
Pulse Generator
7426
beam
7410
fc/n
LO
7409
7418
+
7421
Detector
7420
7415
Delay
7412
7419
7422
Controller
7424
7424b
7425
Pulse Generator
7414
7402
7413
7416
UFT
7423
7415

FIG. 74

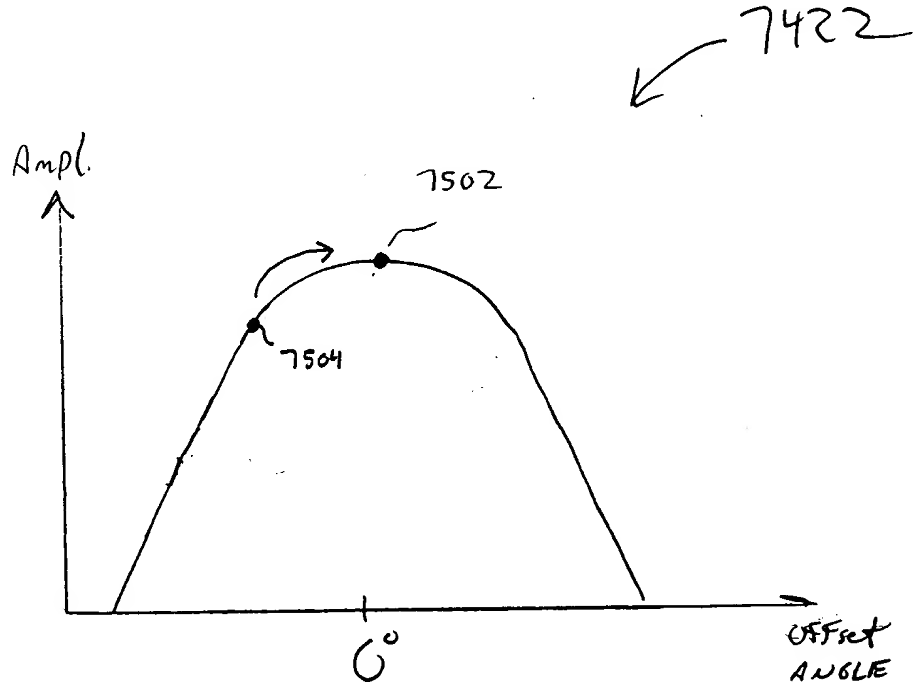


FIG. 75

00609 0"SS606S60

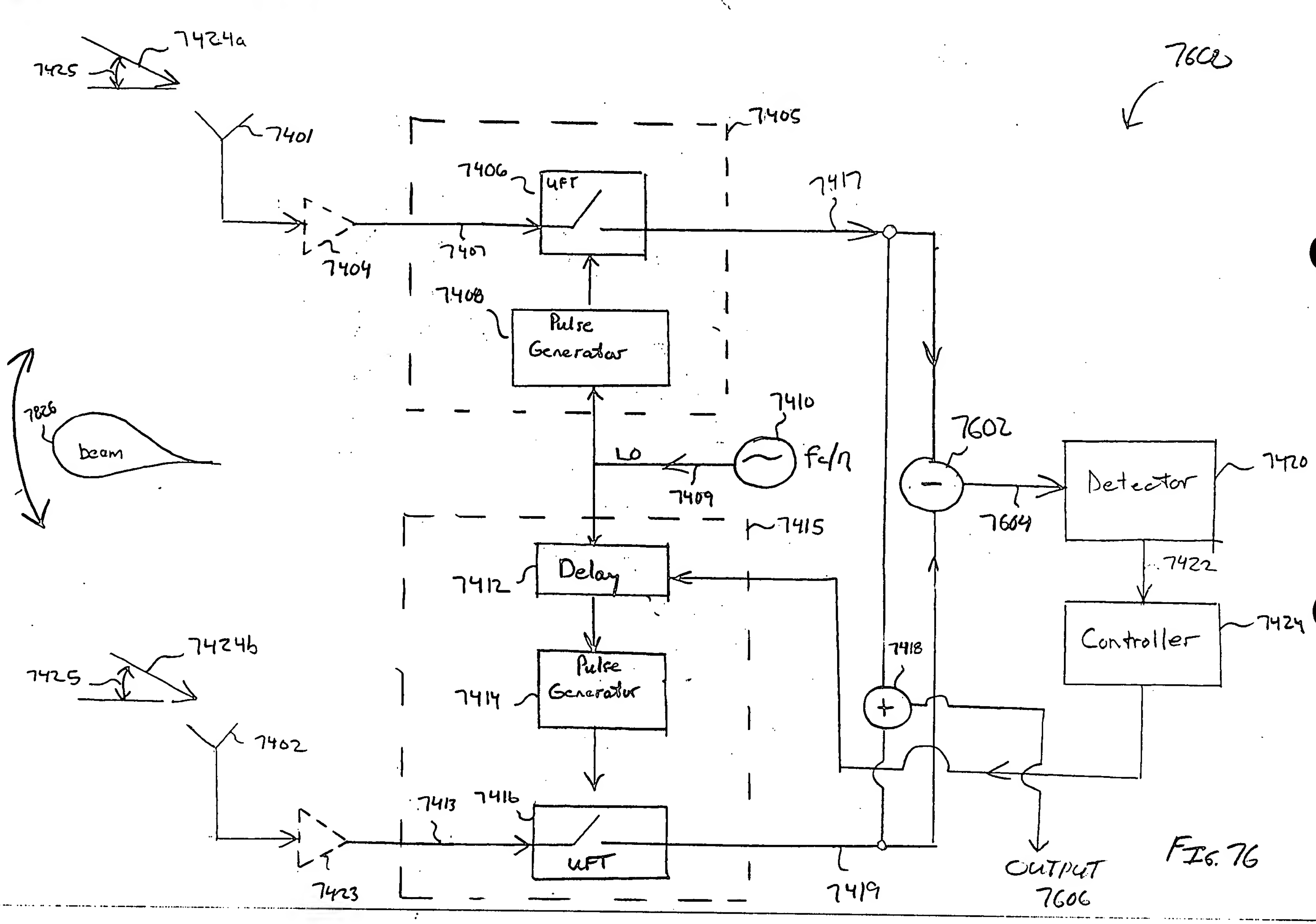


FIG. 76

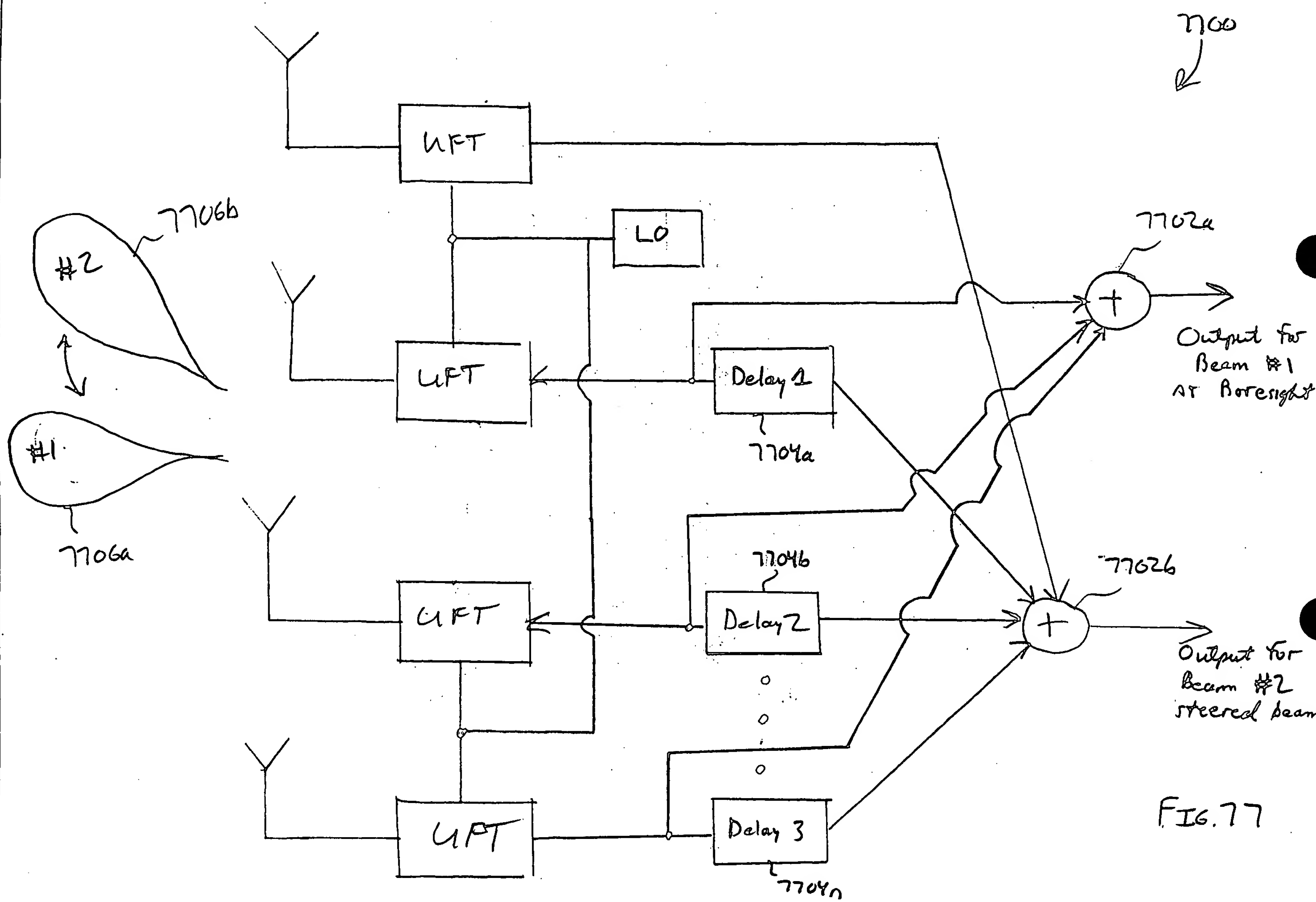

7700
#2
7706b
#1
7706a
UFT
UFT
UFT
UFT
LO
Delay 1
7704a
Delay 2
7704b
Delay 3
7704n
7702a
7702b
Output for
Beam #1
at Boresight
Output for
Beam #2
steered beam

FIG. 77

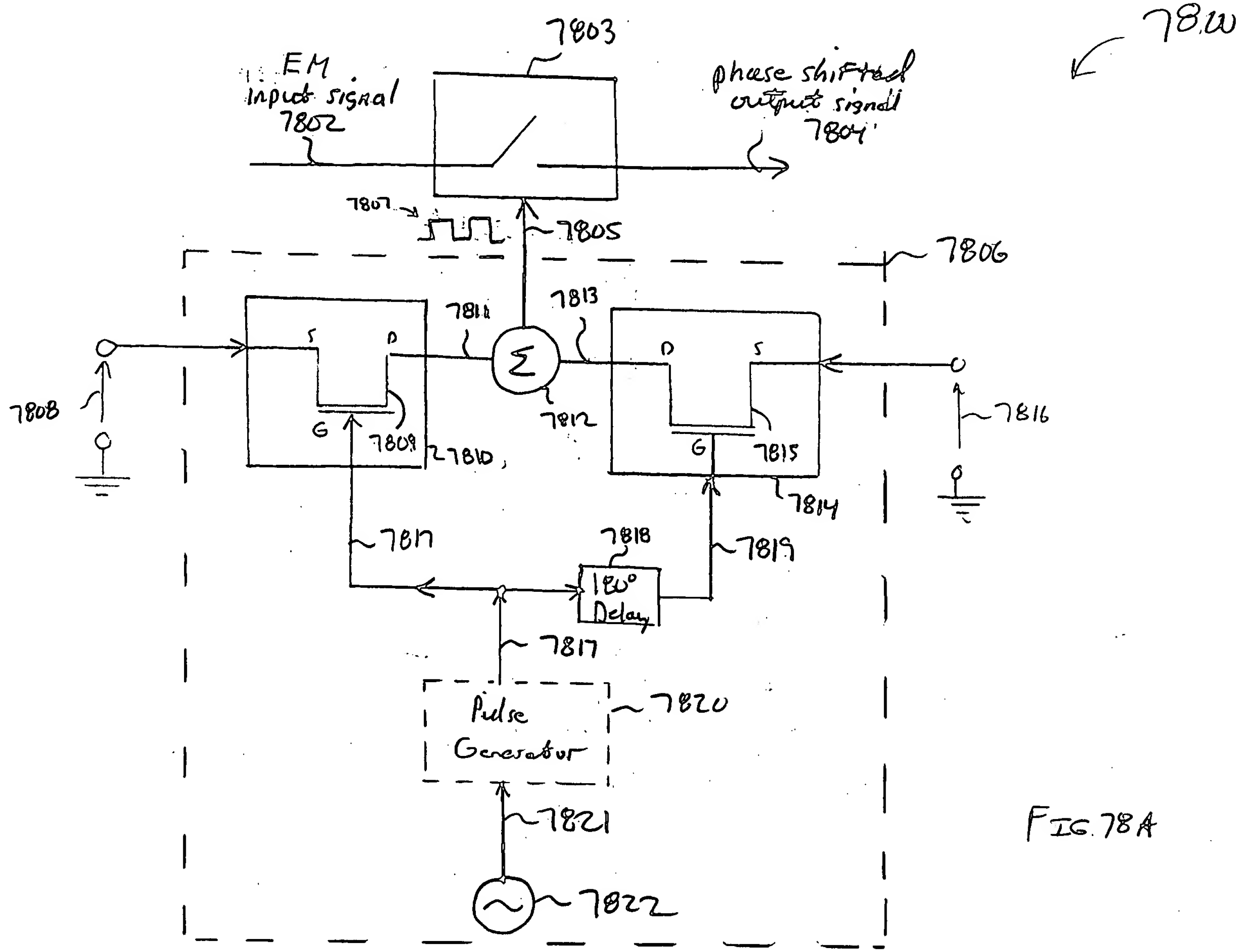

7800
7803
EM
input signal
7802
phase shifted
output signal
7804
7807
7805
7806
7808
S
D
G
7809
7810
7811
7812
7813
D
S
G
7815
7814
7816
7817
7818
180°
Delay
7819
7817
Pulse
Generator
7820
7821
7822

FIG. 78A

FIG. 78B

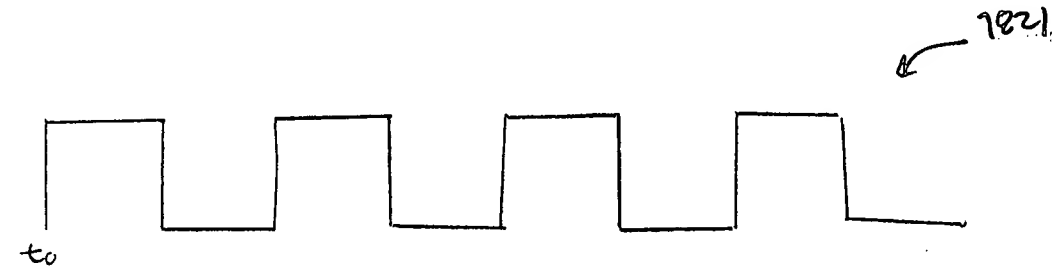


FIG. 78C

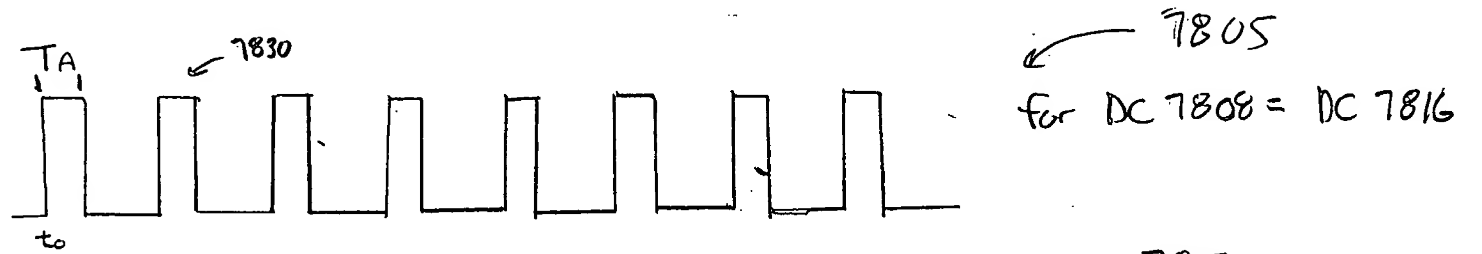
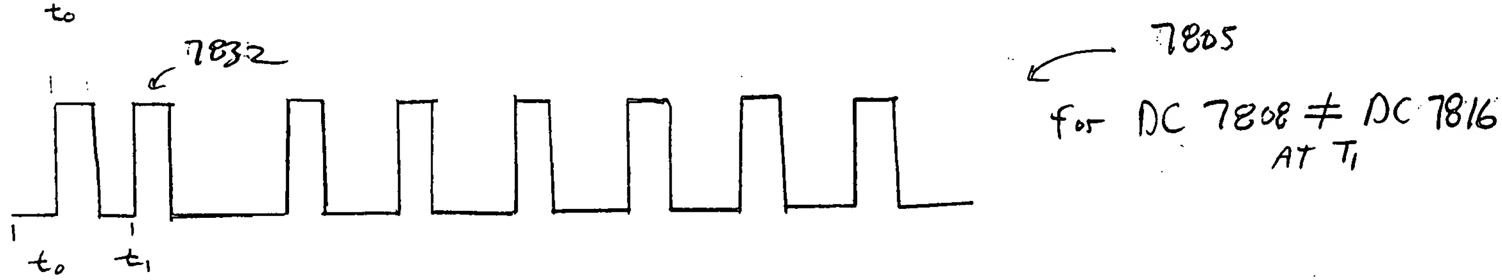


FIG. 78D



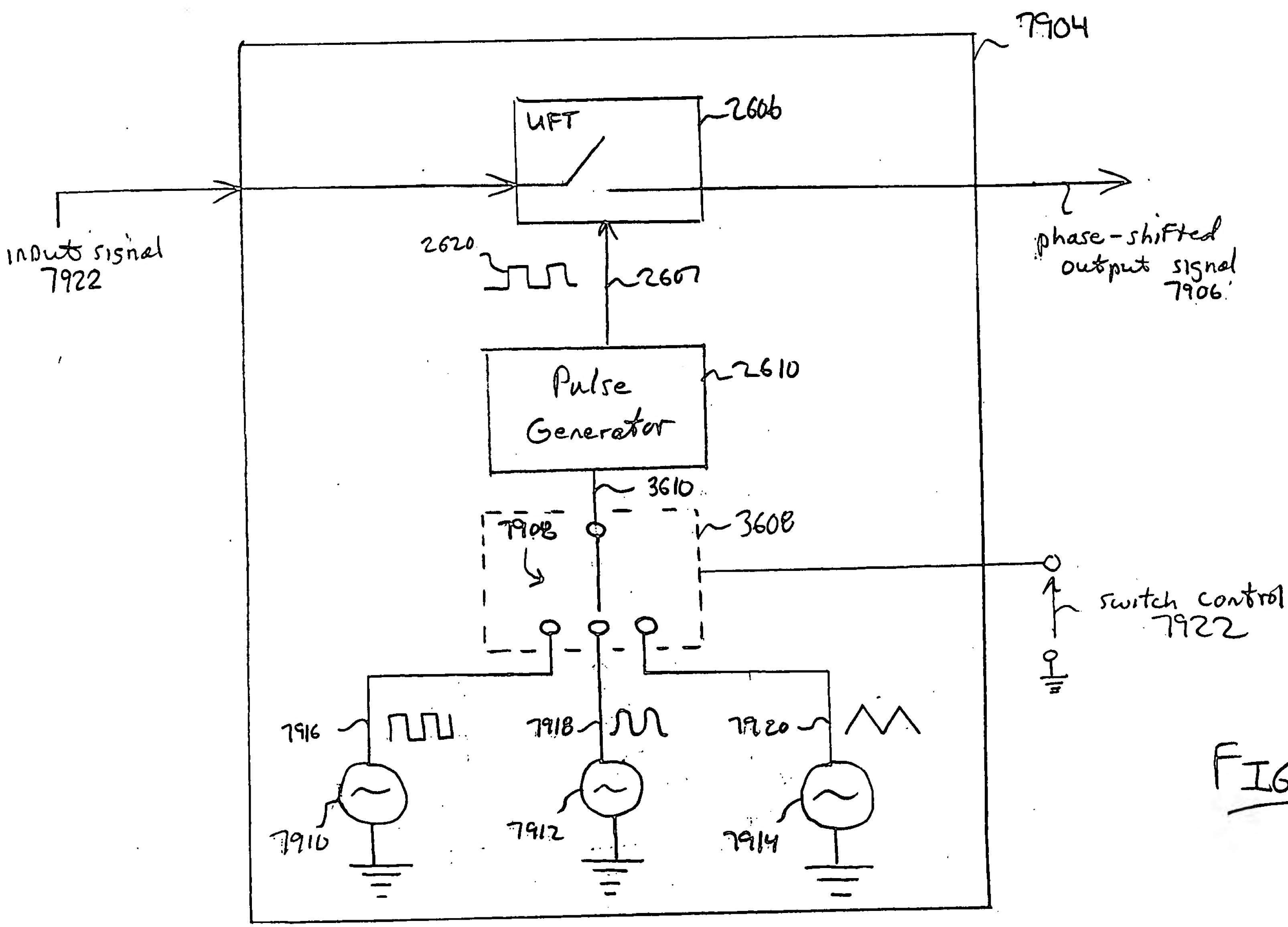

7904
UFT
2606
input signal
7922
phase-shifted
output signal
7906
2620
2607
Pulse
Generator
2610
3610
3608
7908
switch control
7922
7916
7918
7920
7910
7912
7914

FIG. 79

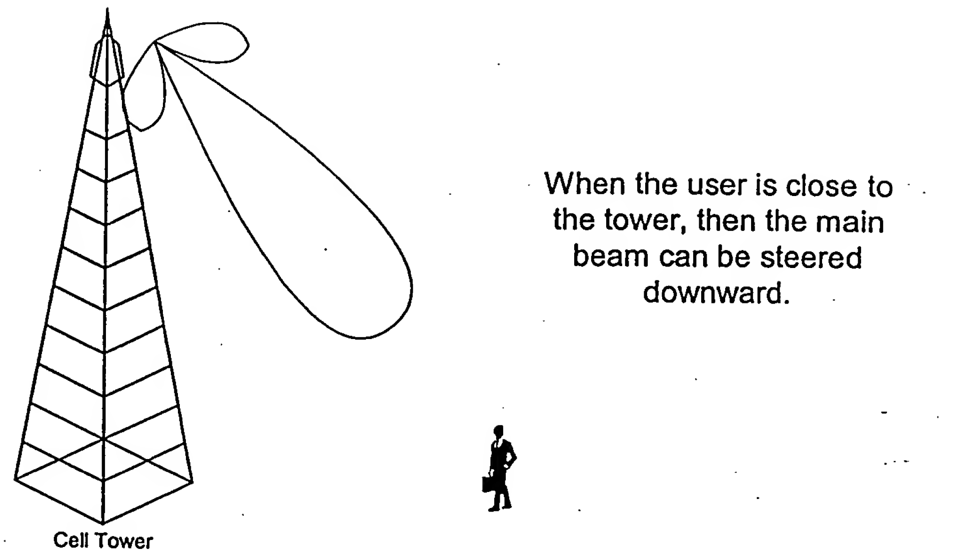


FIG. 80A

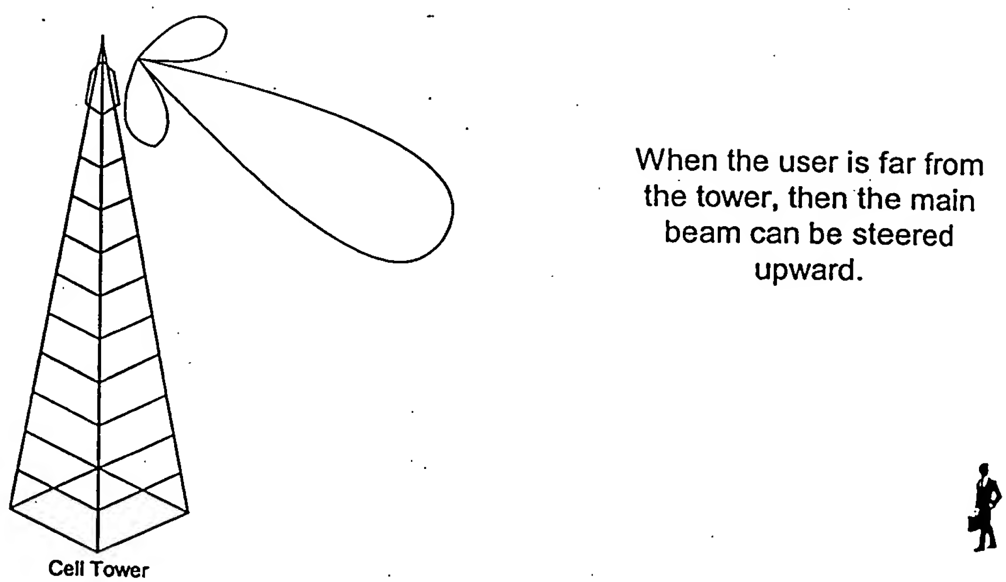


FIG. 80B

00609055606560

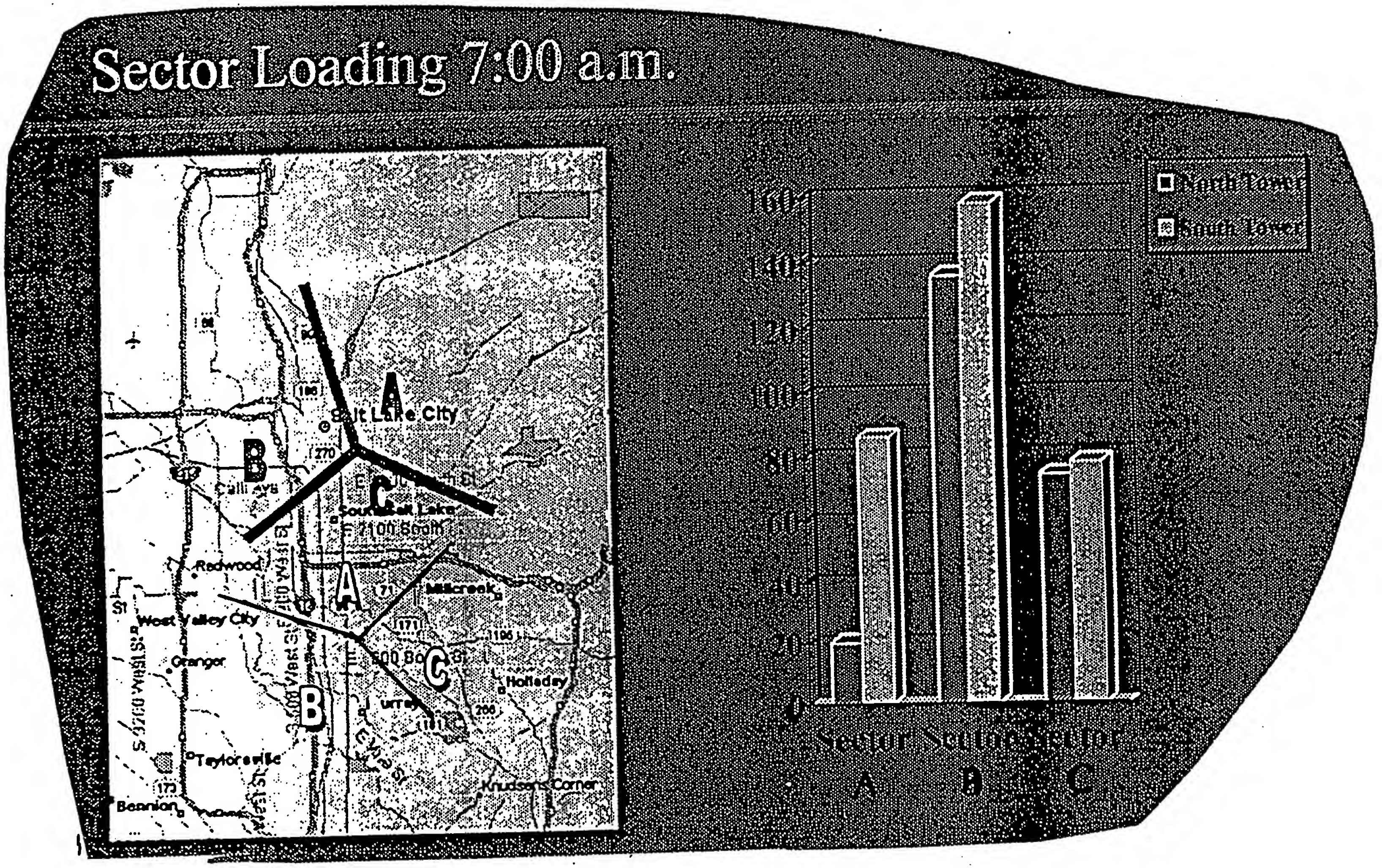


FIG. 81

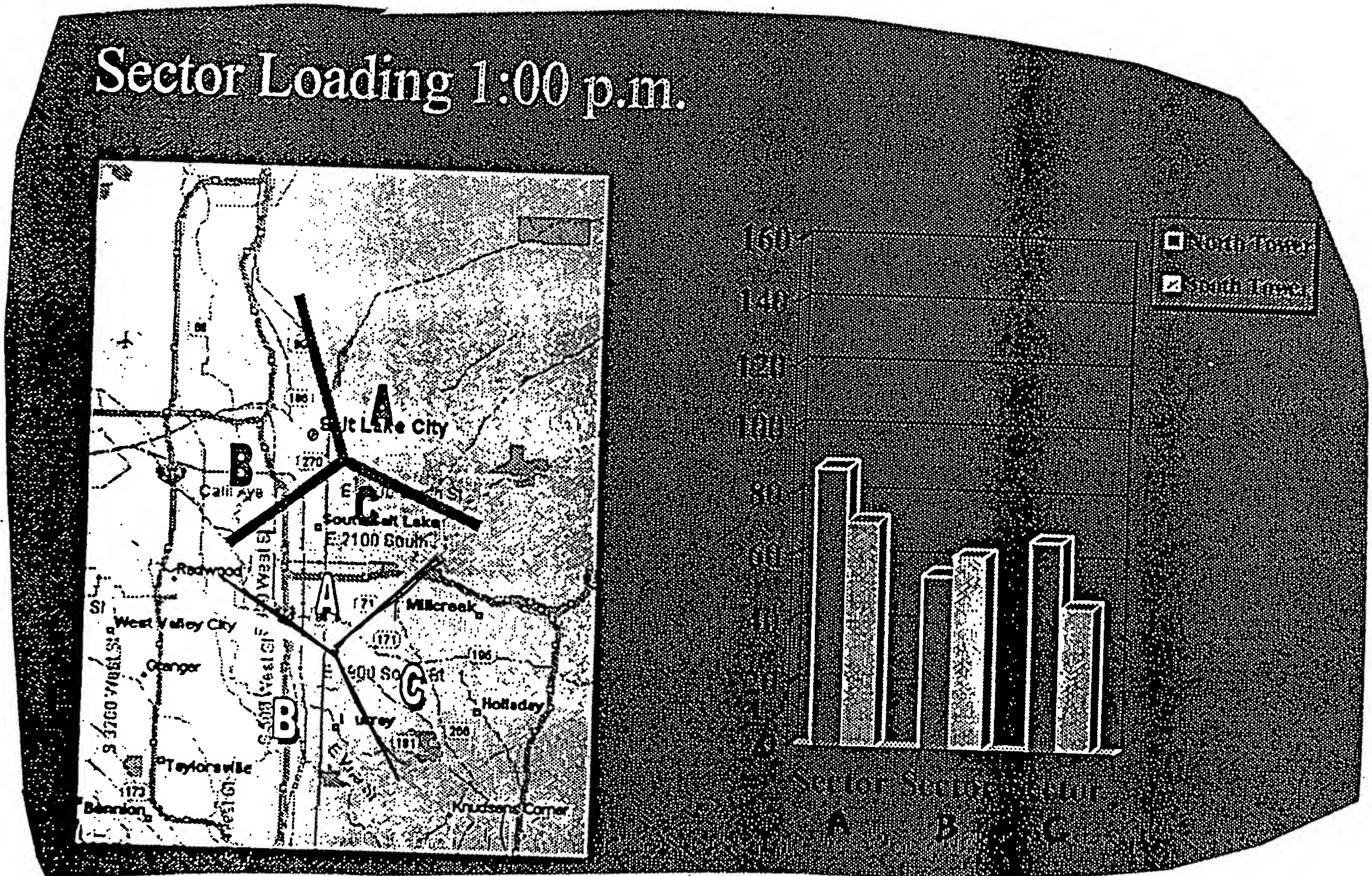

Sector Loading 1:00 p.m.
Salt Lake City
Holladay
Millcreek
West Valley City
Taylorsville
Bennion
Redwood
Knudsens Corner
E 2100 South
160
140
120
100
80
60
40
0
North Tower
South Tower
A
B
C

FIG. 82

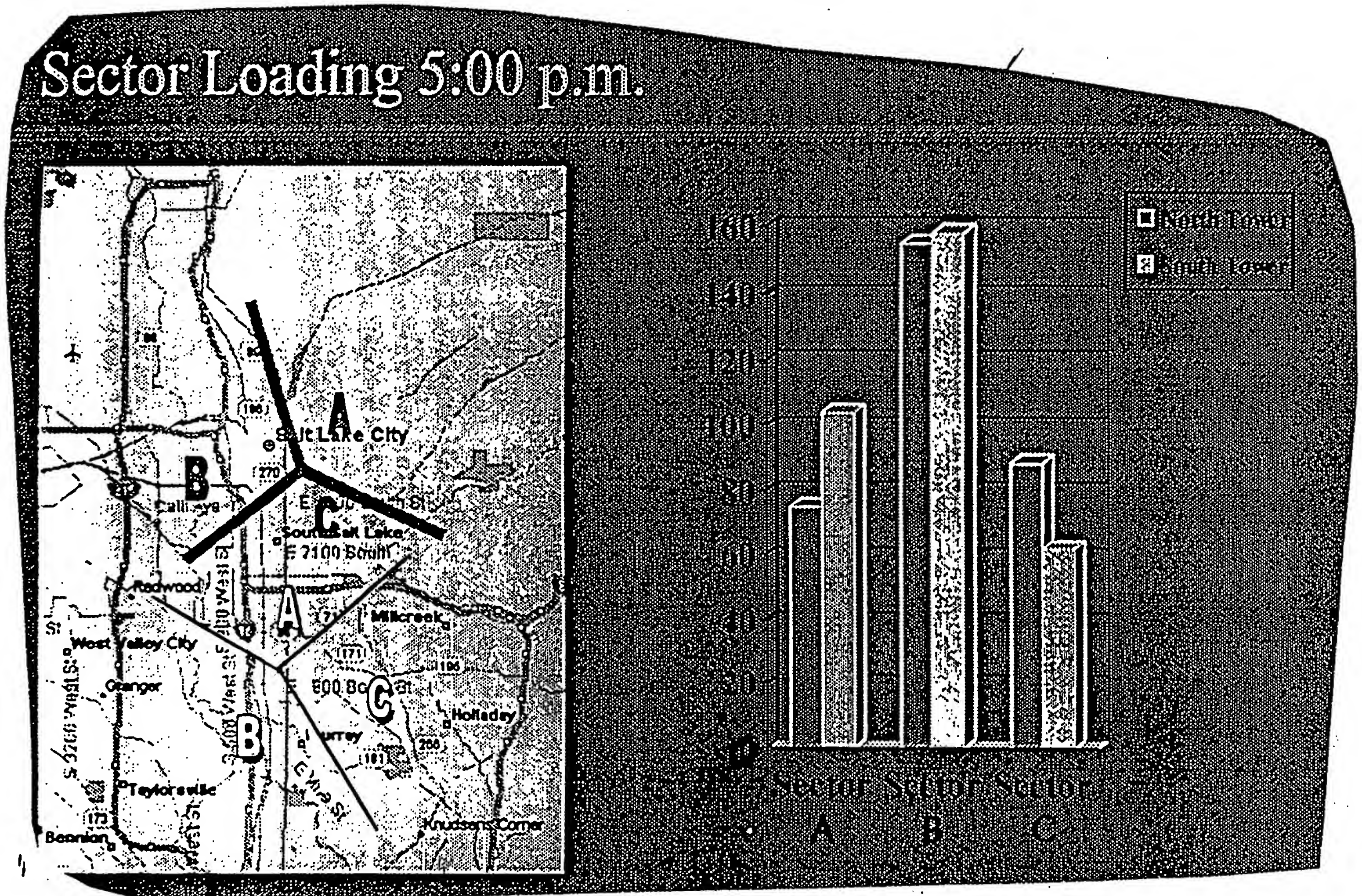

Sector Loading 5:00 p.m.
North Tower
South Tower
160
140
120
100
80
60
40
20
0
Sector A
Sector B
Sector C
A
B
C
Salt Lake City
South Salt Lake
E 2100 South
Redwood
Millcreek
West Valley City
Granger
Holladay
Taylorsville
Knudsens Corner
Bennion

FIG. 83

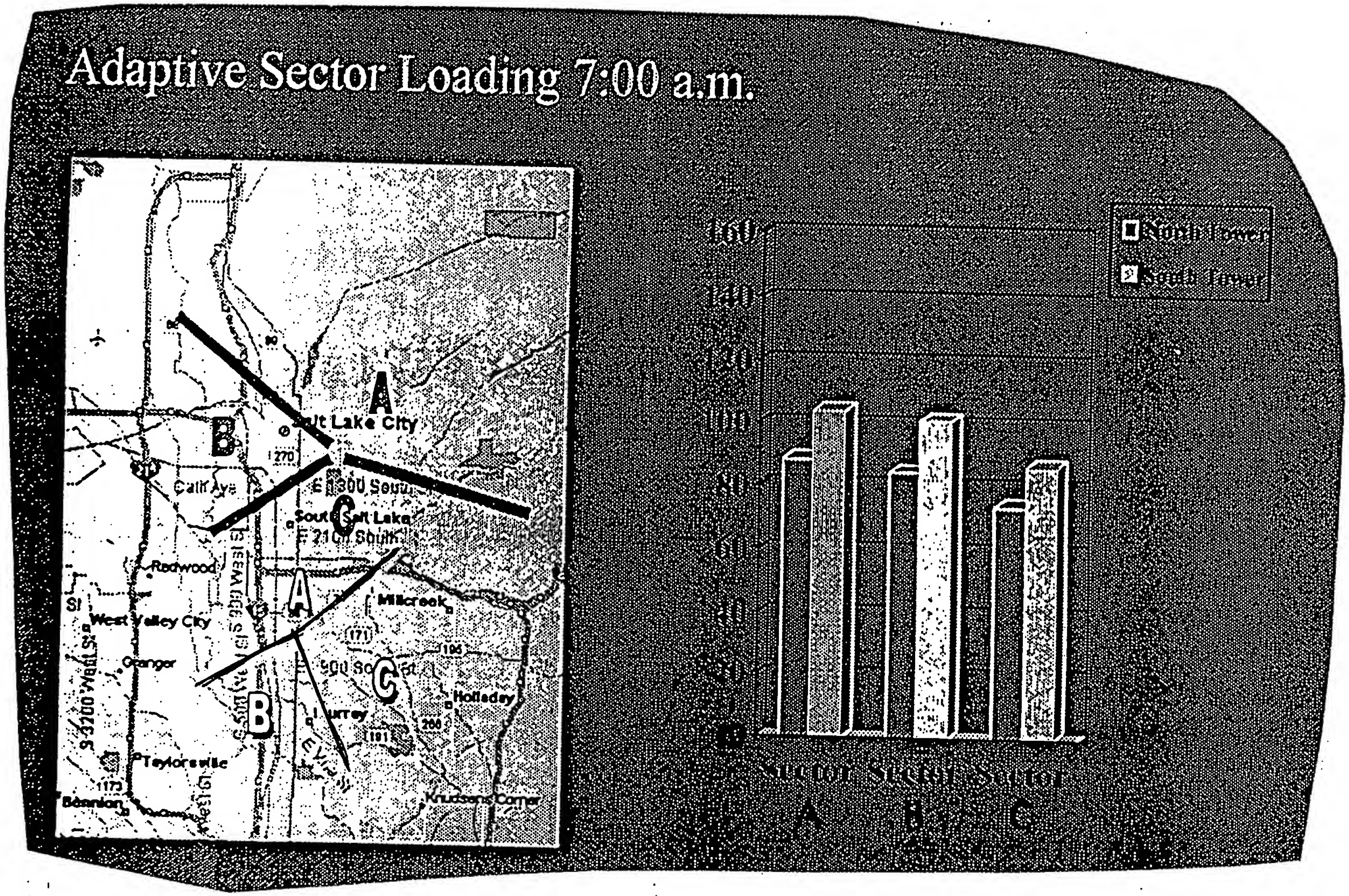

Adaptive Sector Loading 7:00 a.m.
North Tower
South Tower
160
140
120
100
80
60
40
20
0
Sector A
Sector B
Sector C
A
B
C
Salt Lake City
South Salt Lake
Calif Ave
Redwood
West Valley City
Granger
Millcreek
Holladay
Murray
Taylorsville
Bennion
Knudsens Corner

FIG. 84

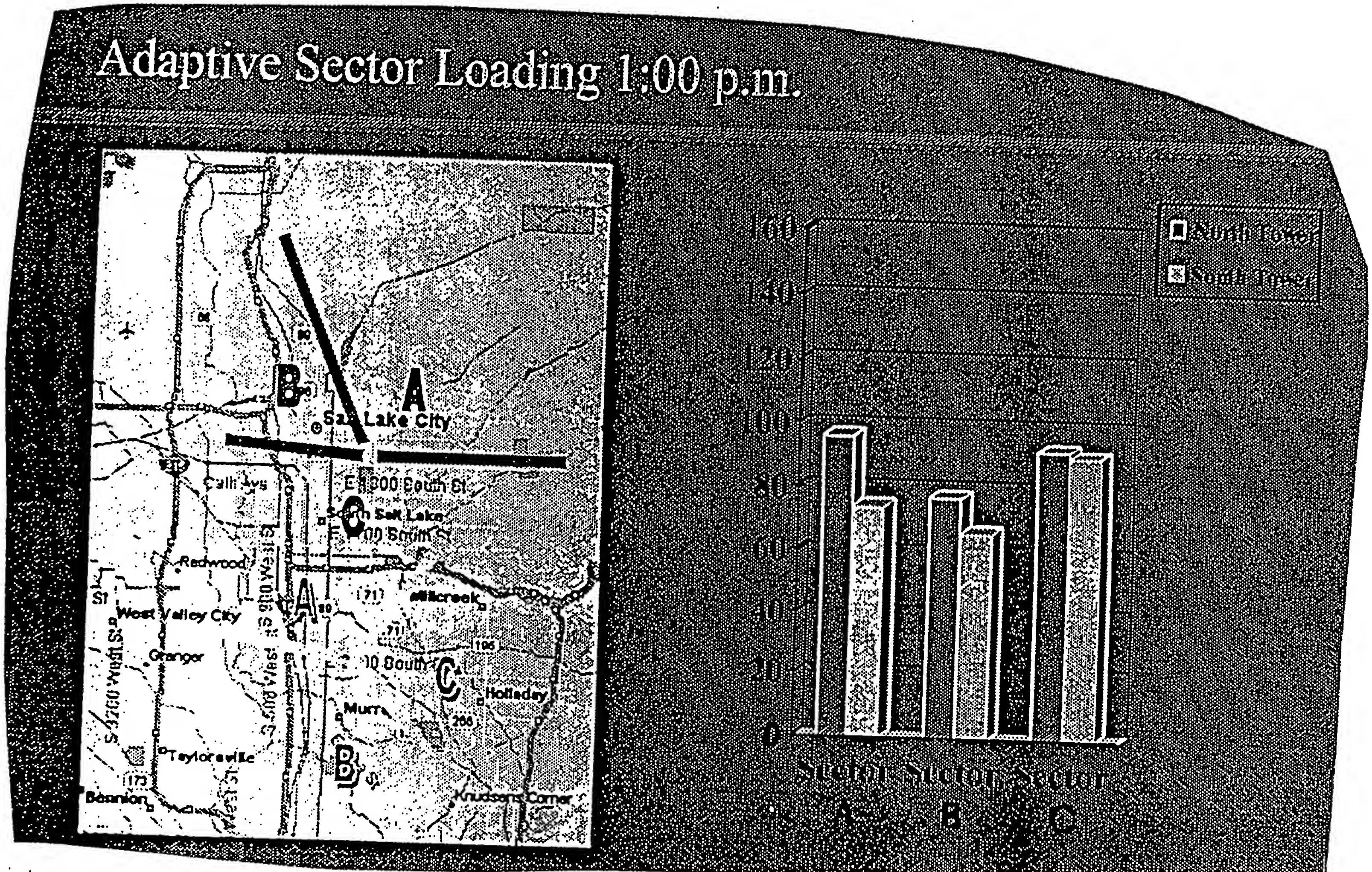

Adaptive Sector Loading 1:00 p.m.
Salt Lake City
A
B
C
Redwood
West Valley City
Granger
Taylorsville
Bennion
Millcreek
Holladay
Murray
Knudsens Corner
160
140
120
100
80
60
40
20
0
North Tower
South Tower
Sector A
Sector B
Sector C

FIG. 85

006090"55606560

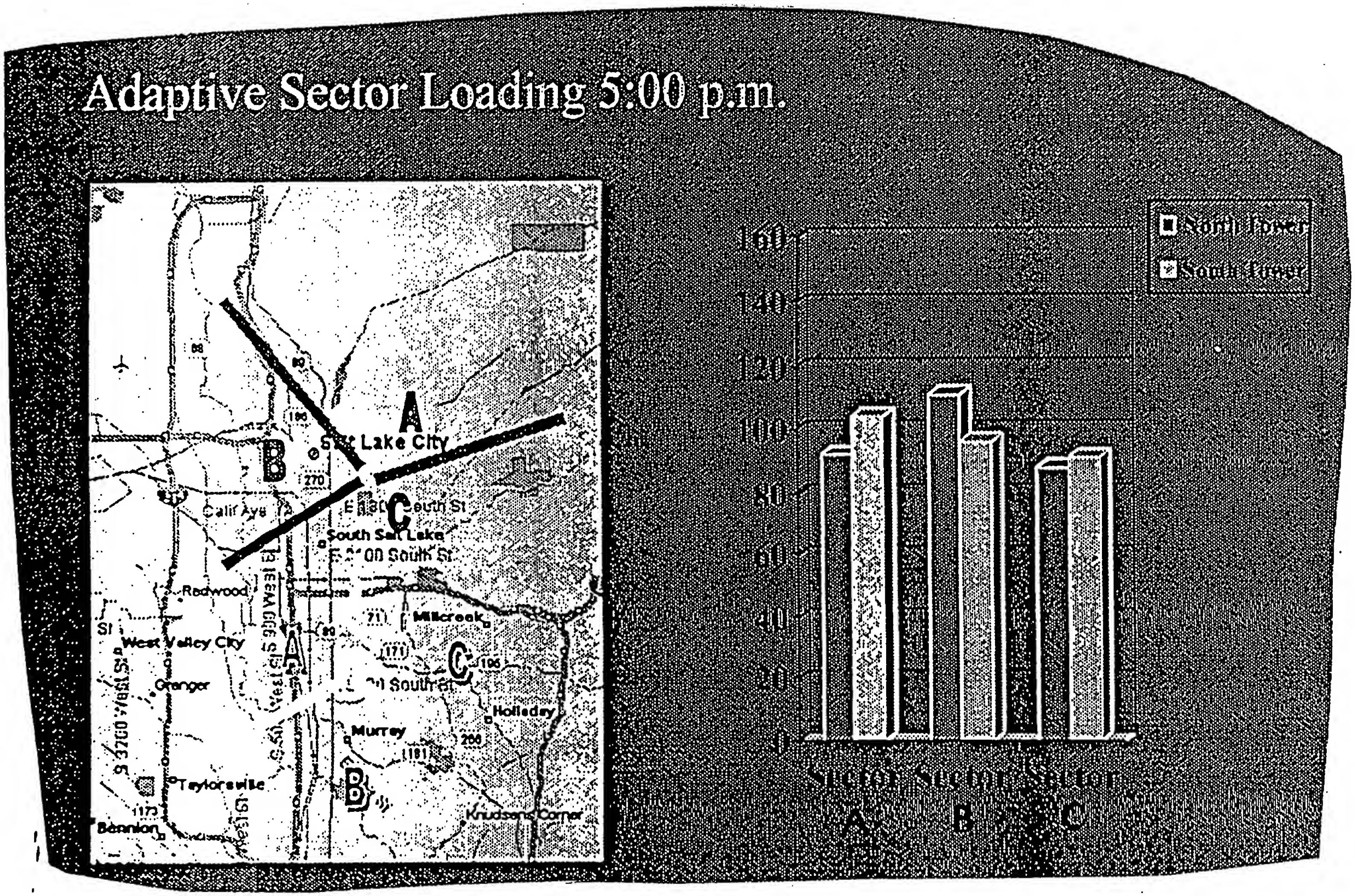


FIG. 86

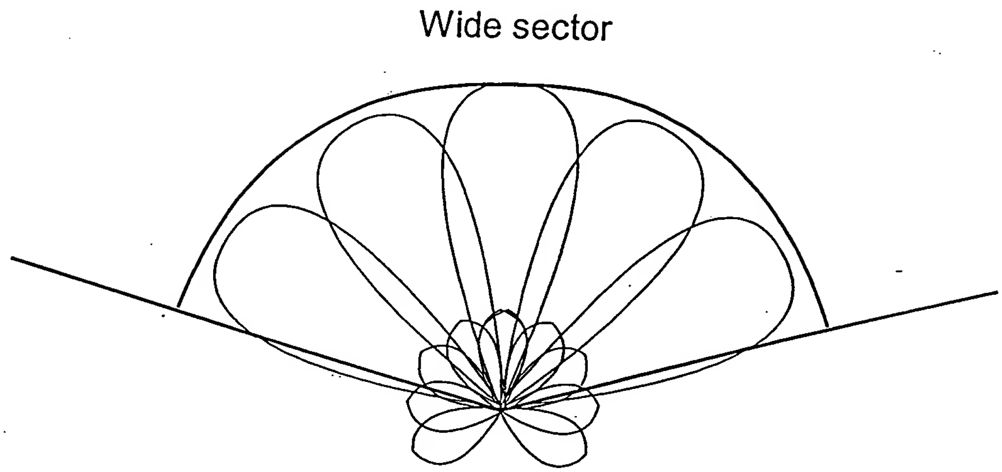


FIG. 87A

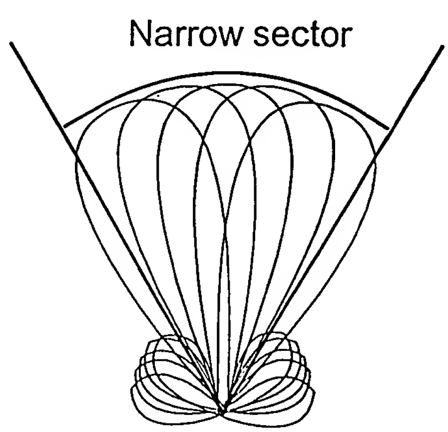


FIG. 87B

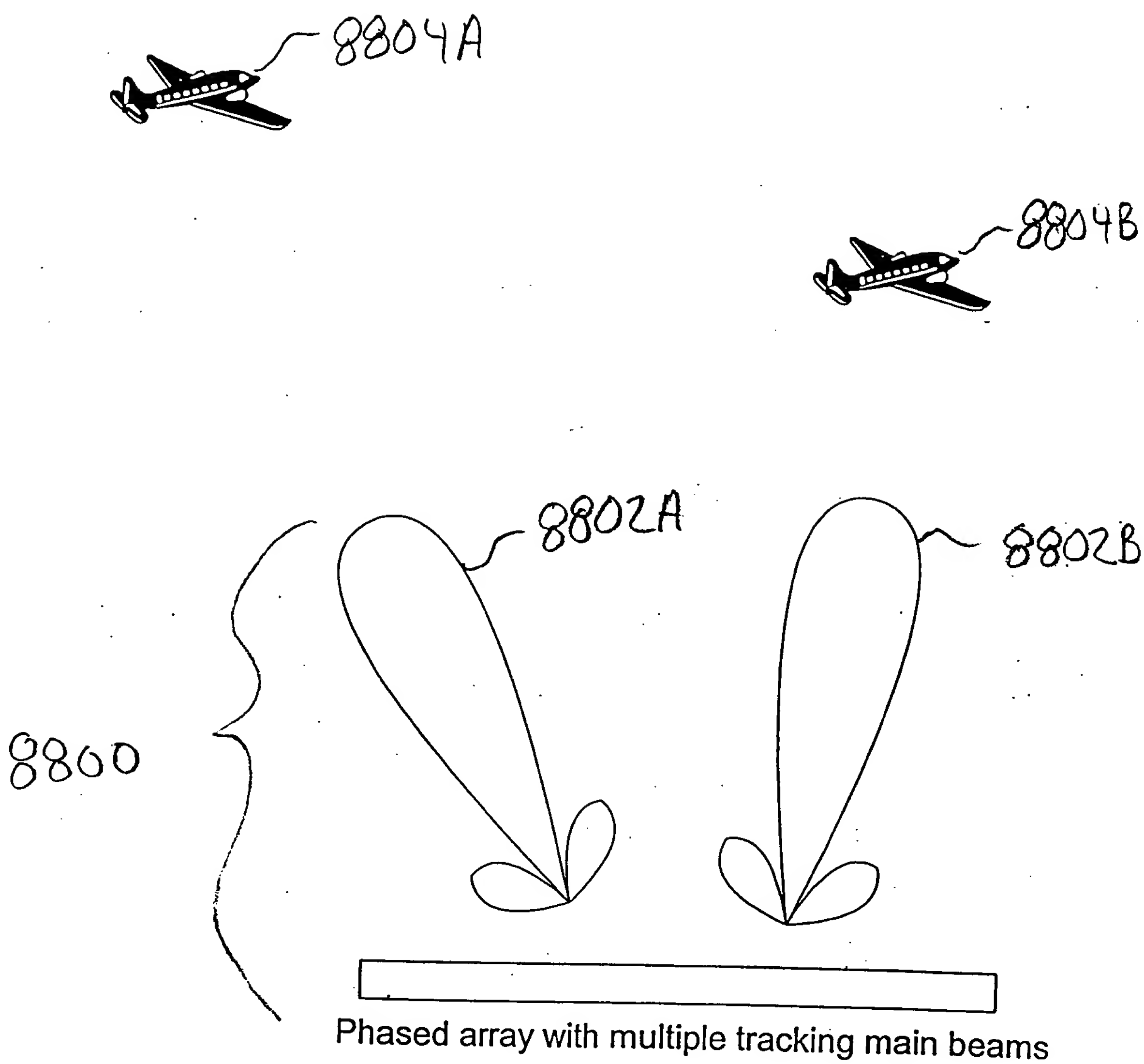

8804A
8804B
8802A
8802B
8800
Phased array with multiple tracking main beams

FIG. 88

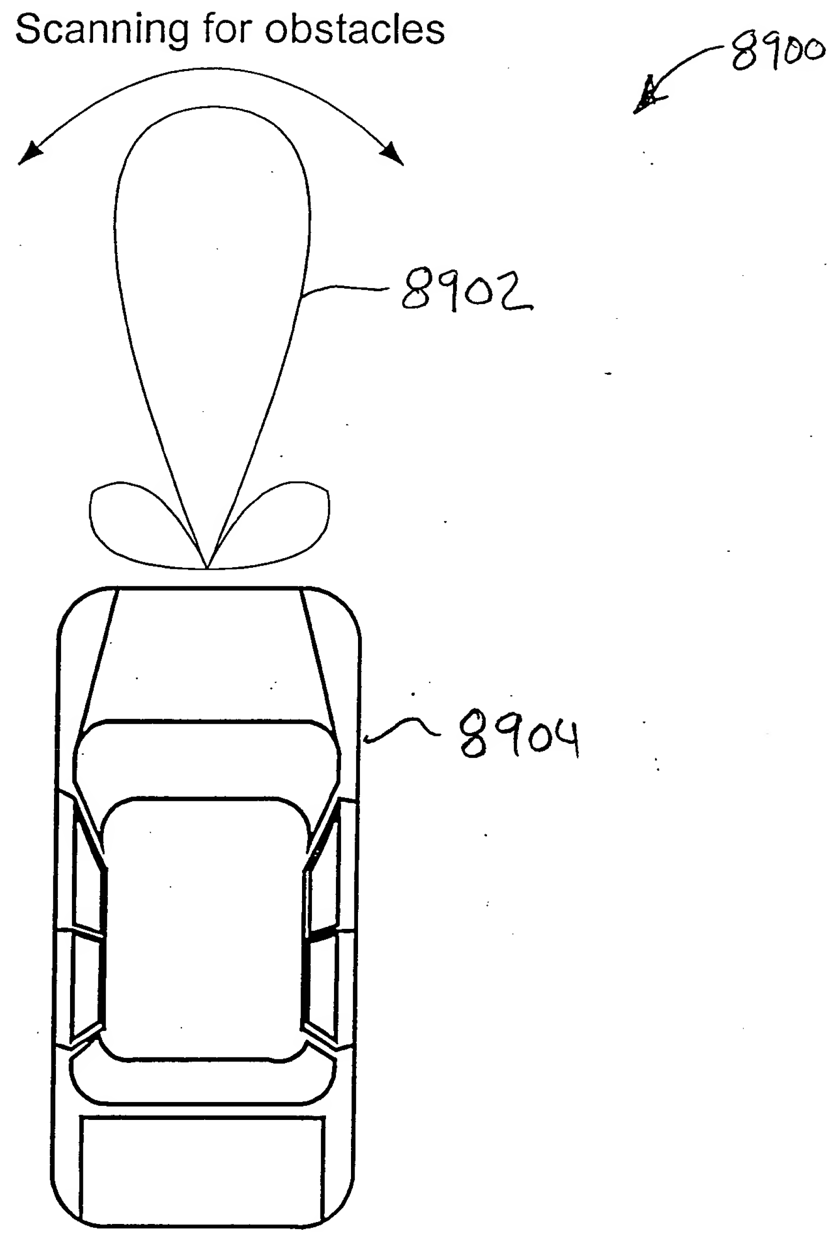


FIG. 89

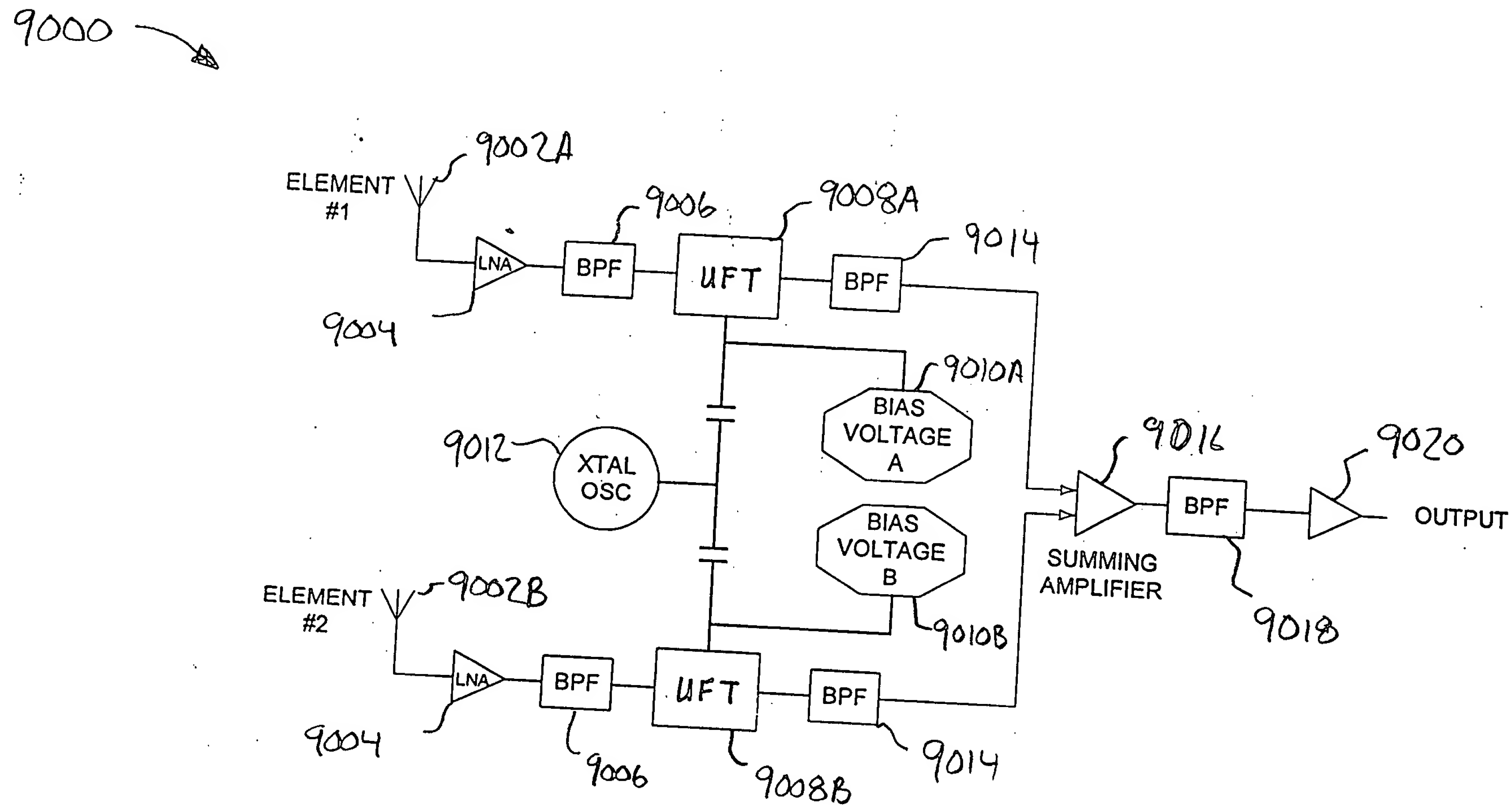

9000
ELEMENT #1
9002A
9004
9006
BPF
UFT
9008A
BPF
9014
LNA
9010A
BIAS VOLTAGE A
9012
XTAL OSC
BIAS VOLTAGE B
9010B
ELEMENT #2
9002B
LNA
9004
BPF
9006
UFT
9008B
BPF
9014
9016
SUMMING AMPLIFIER
BPF
9018
9020
OUTPUT

FIG. 90A

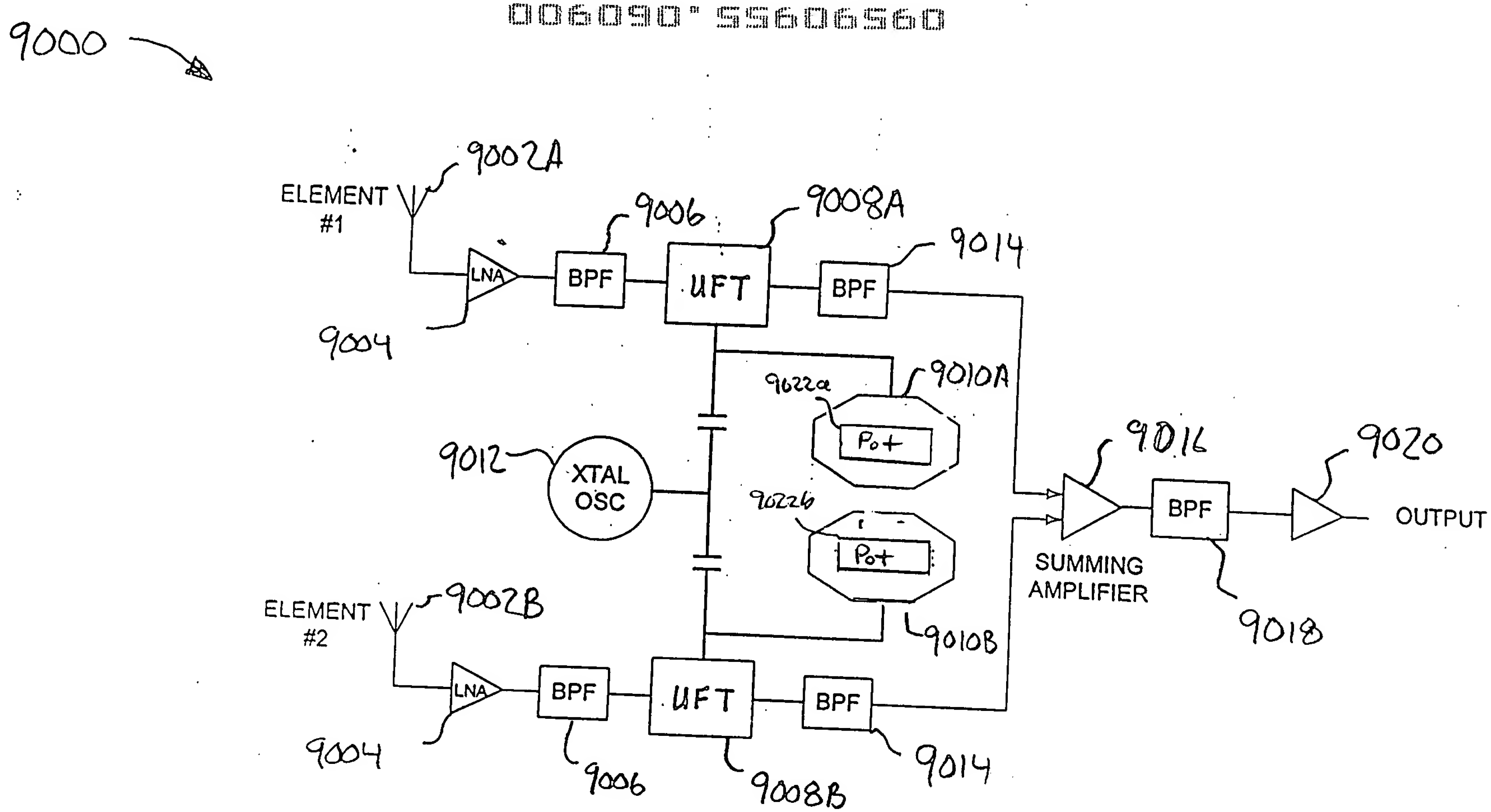

9000
ELEMENT #1
9002A
LNA
9004
BPF
9006
UFT
9008A
BPF
9014
9022a
9010A
Po+
9012
XTAL OSC
9022b
Po+
9010B
ELEMENT #2
9002B
LNA
9004
BPF
9006
UFT
9008B
BPF
9014
9016
SUMMING AMPLIFIER
BPF
9018
9020
OUTPUT

FIG. 90B

00609055606560

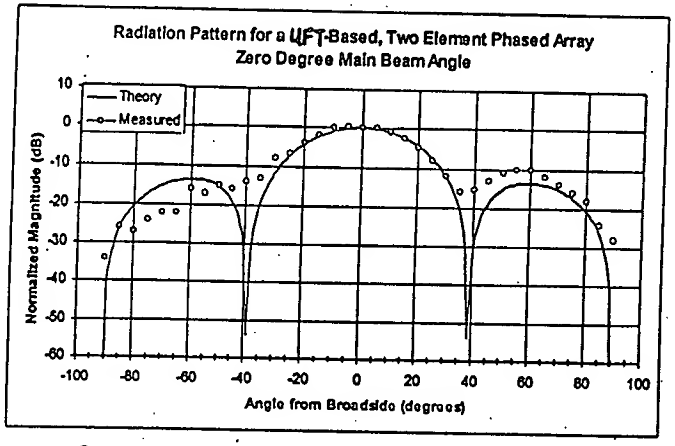


FIG. 91A 0 degree scan angle.

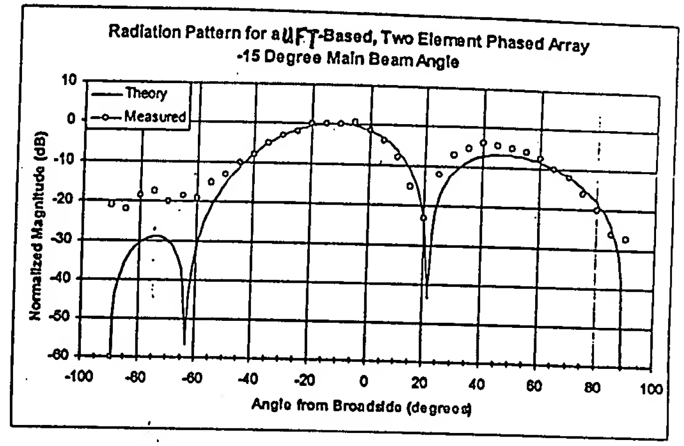


FIG. 91B -15 degree scan angle.

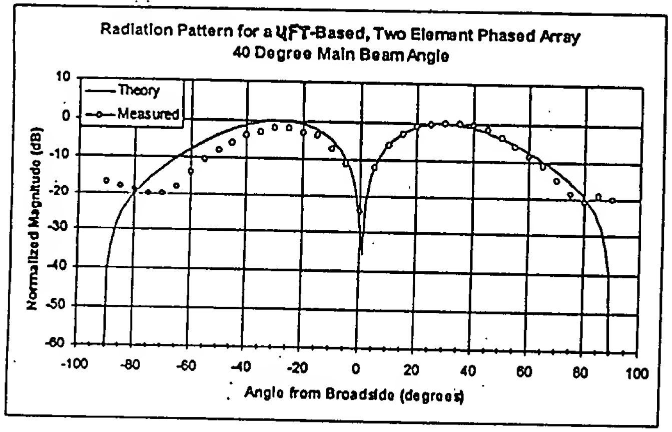


FIG. 91C 40 degree scan angle.

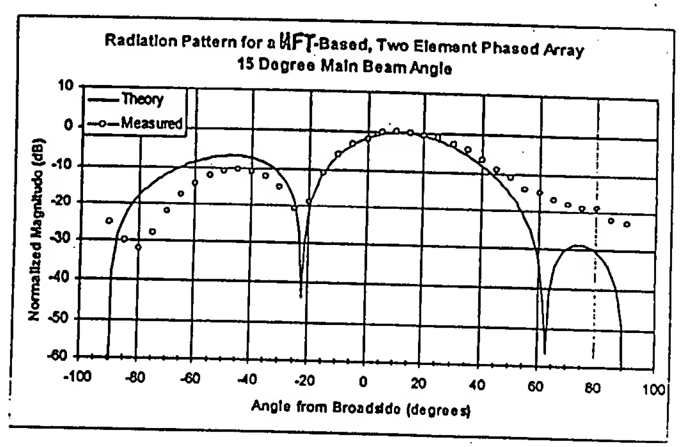


FIG. 91D 15 degree scan angle.

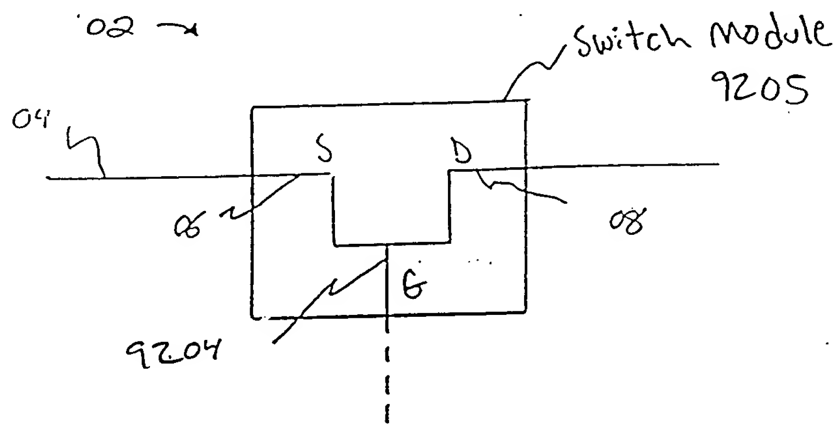


FIG. 92A

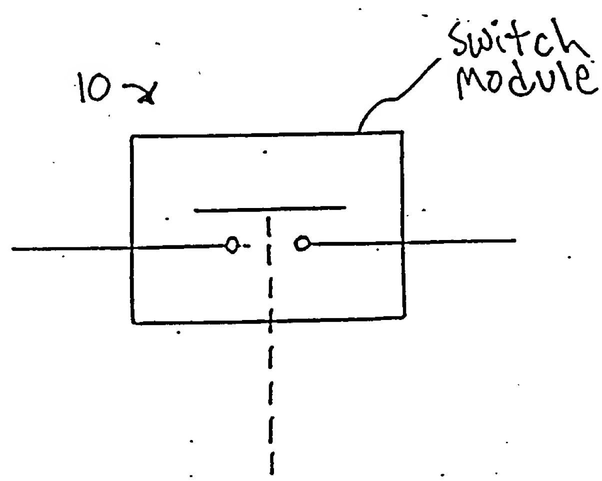


FIG. 92B

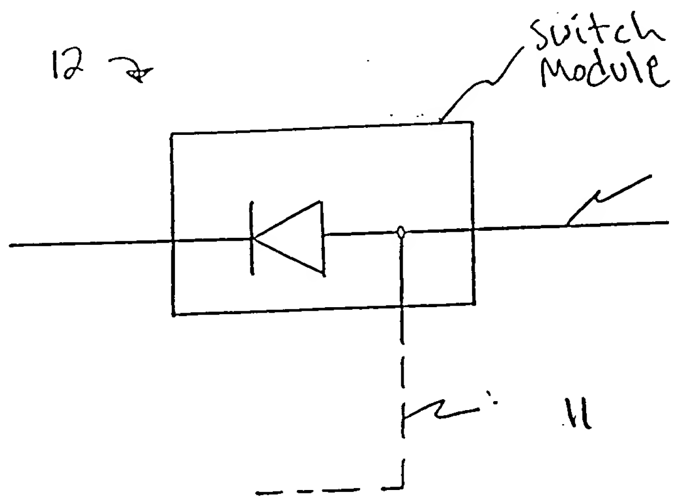


FIG. 92C

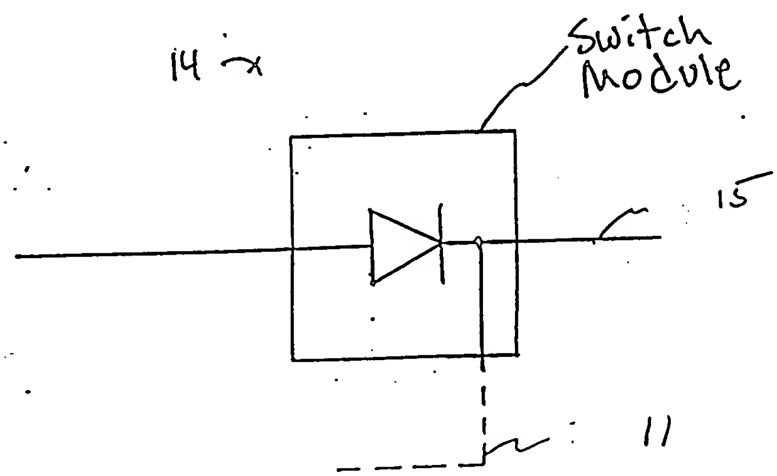
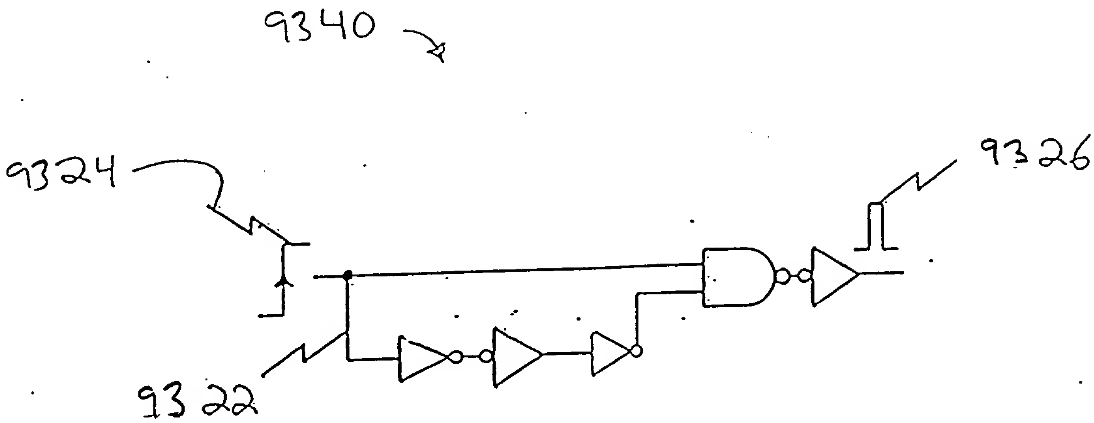
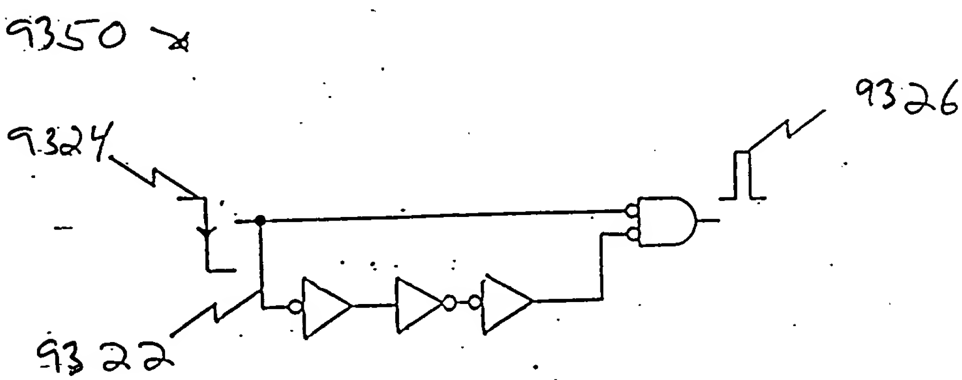


FIG. 92D



A. rising edge pulse generator

FIG. 93A

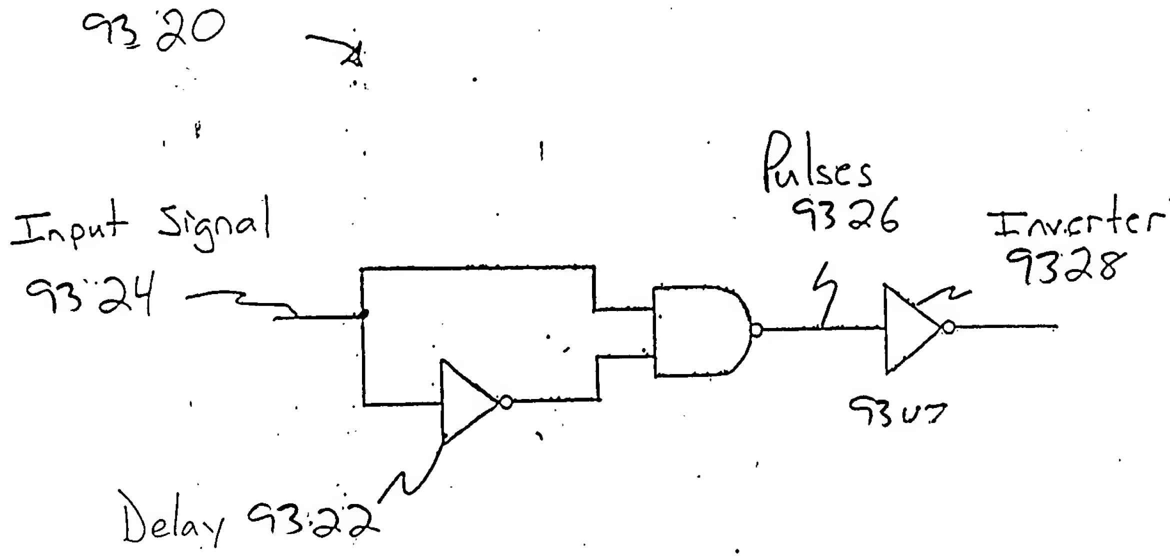


B. falling-edge pulse generator

FIG. 93B

5

5



-substantial equivalence in logic only is necessary.
-u7 shown for polarity consistency with
ckt examples described elsewhere.

FIG 93C

5

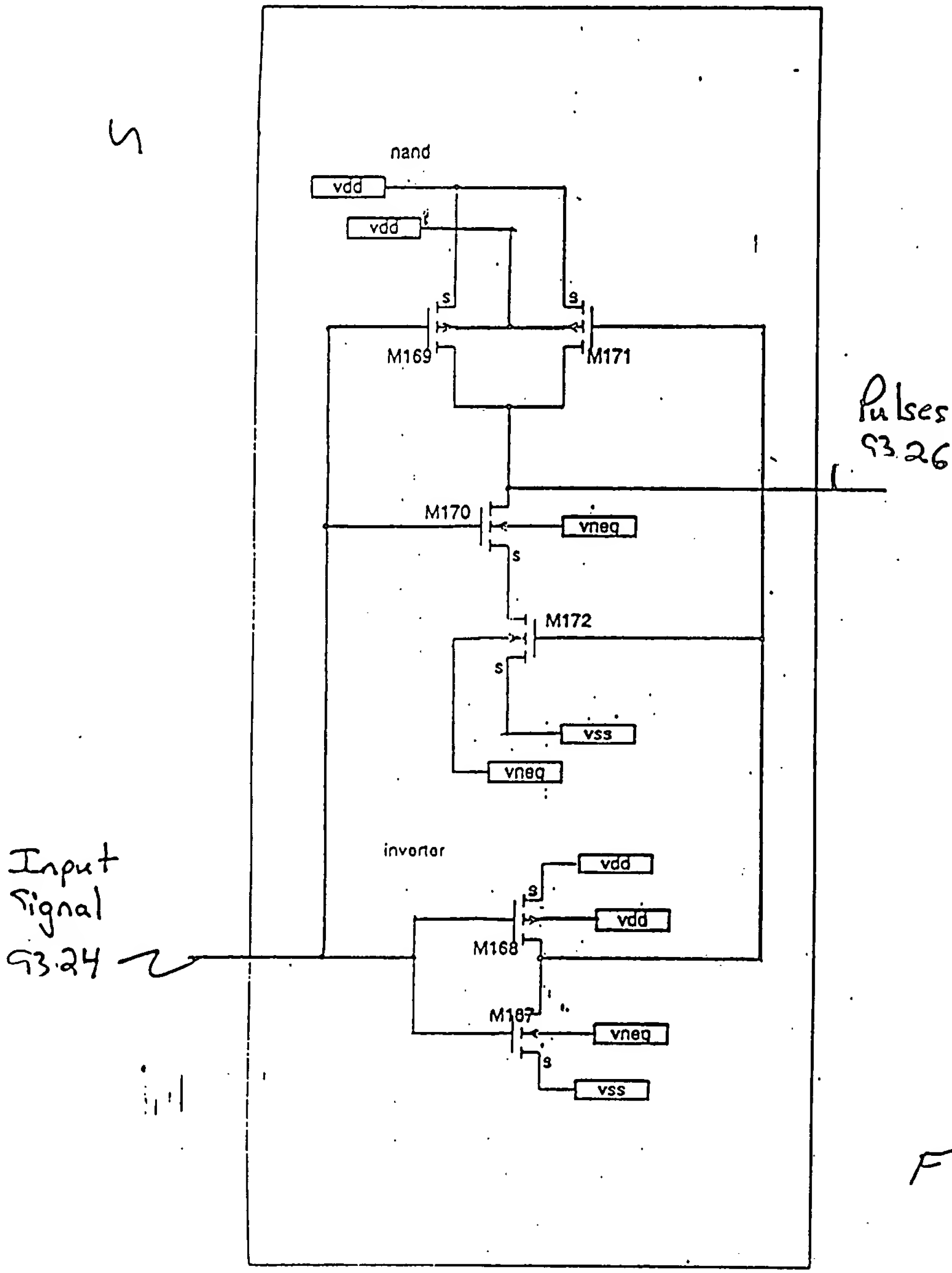


FIG 93D

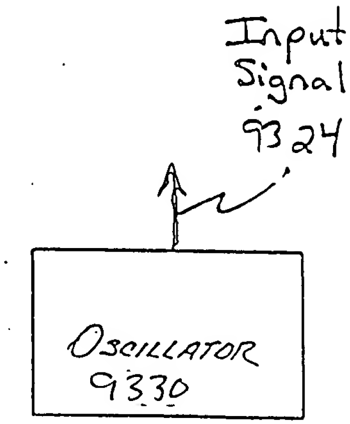


FIG. 93E

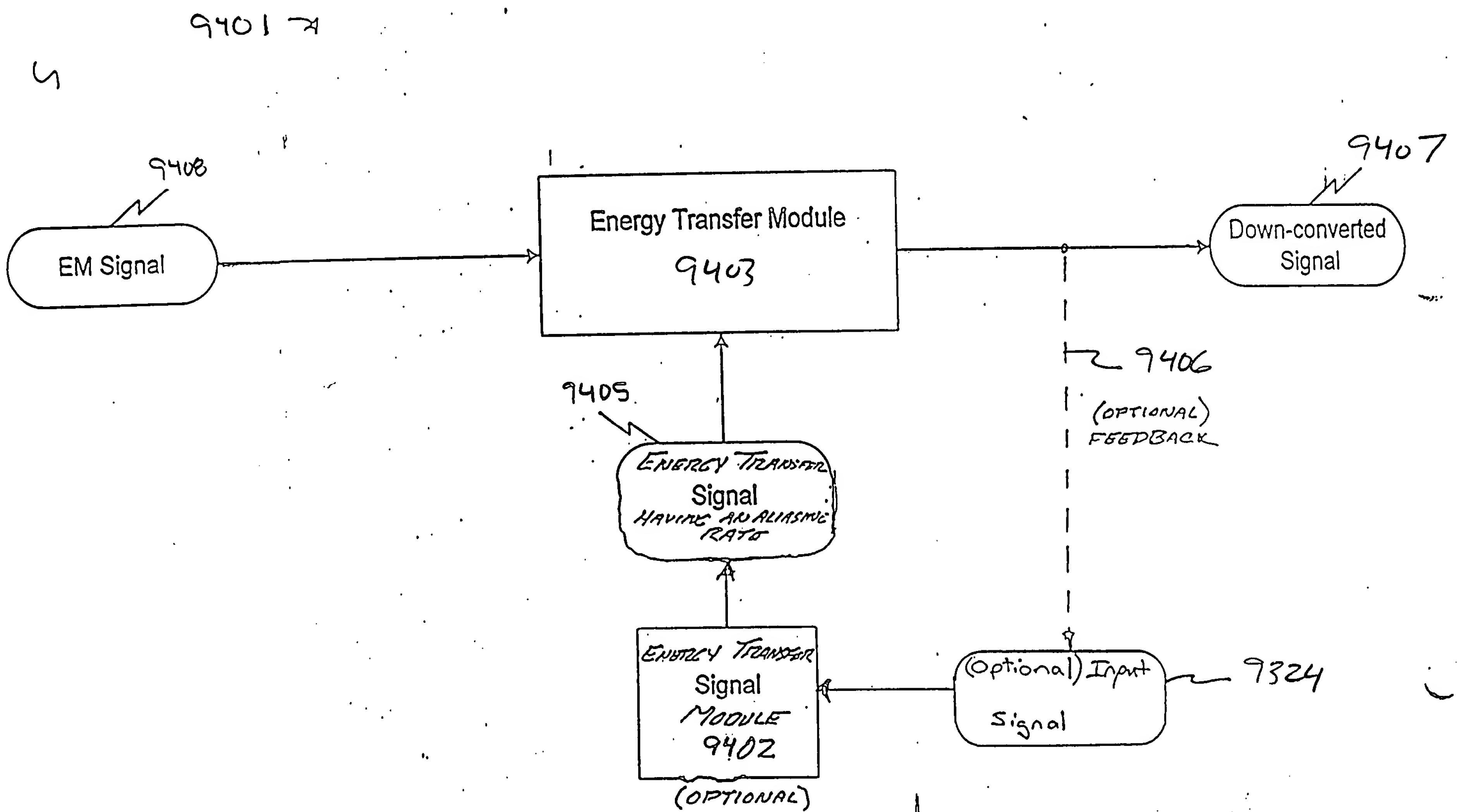

9401
9408
EM Signal
Energy Transfer Module
9403
9407
Down-converted Signal
9406
(OPTIONAL) FEEDBACK
9405
ENERGY TRANSFER Signal HAVING AN ALIASING RATE
ENERGY TRANSFER Signal MODULE 9402
(OPTIONAL)
(Optional) Input Signal
9324

FIG. 94

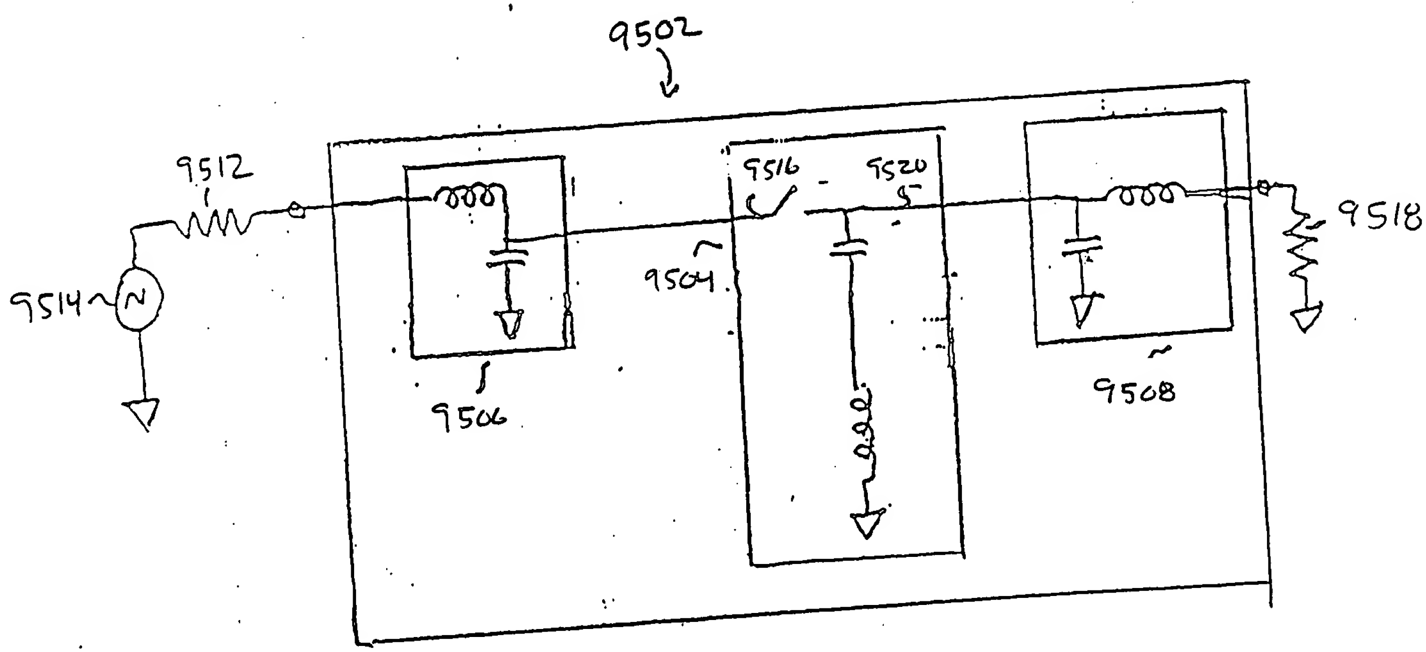


Fig 95 - Impedance Matched Aliasing Module

006090" SS606S60

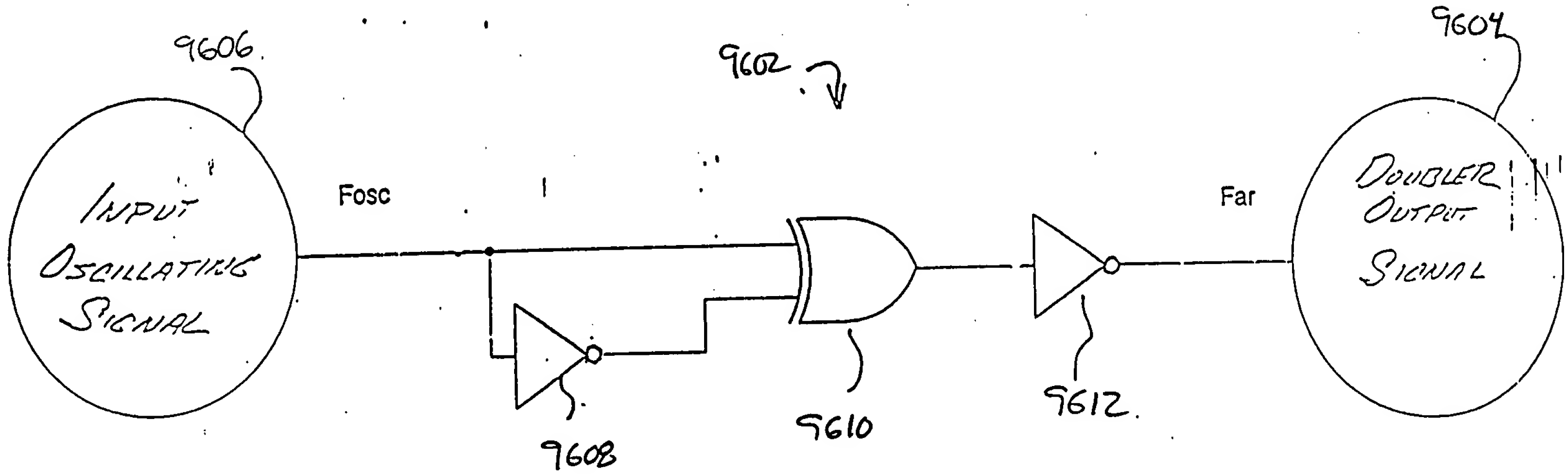


FIG. 96A

FIG. 96B

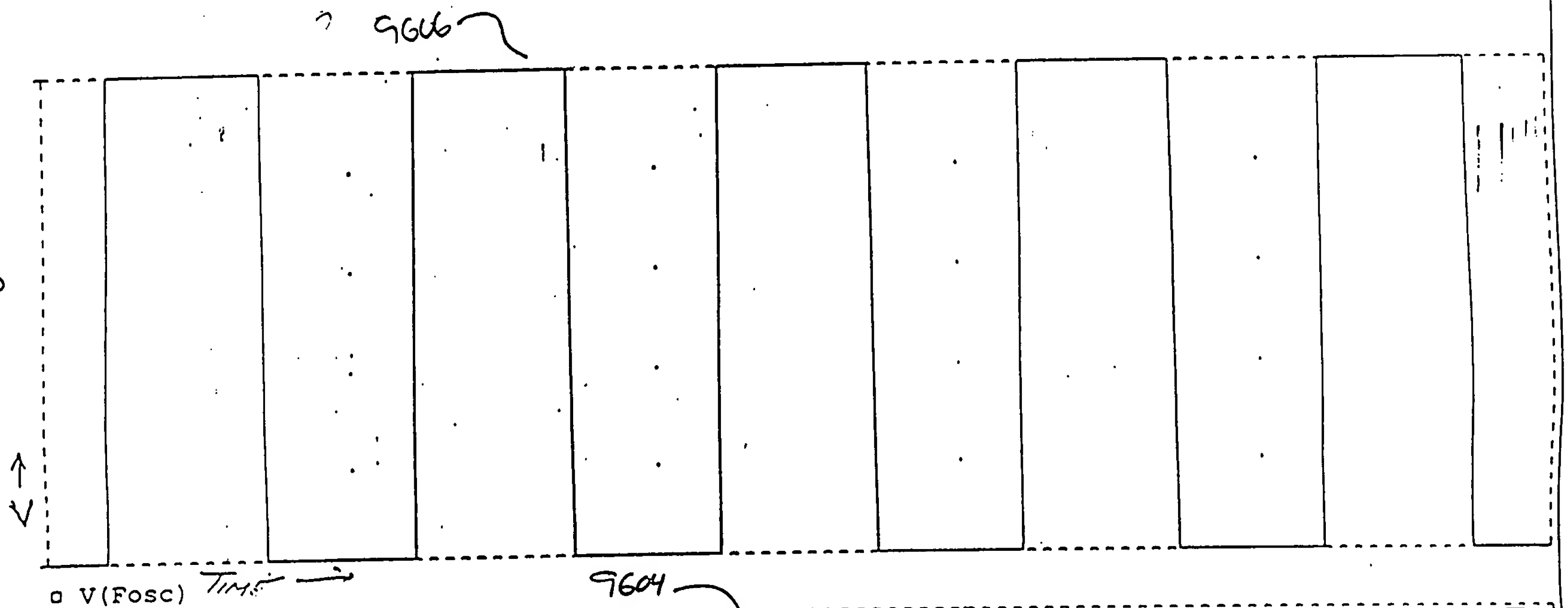
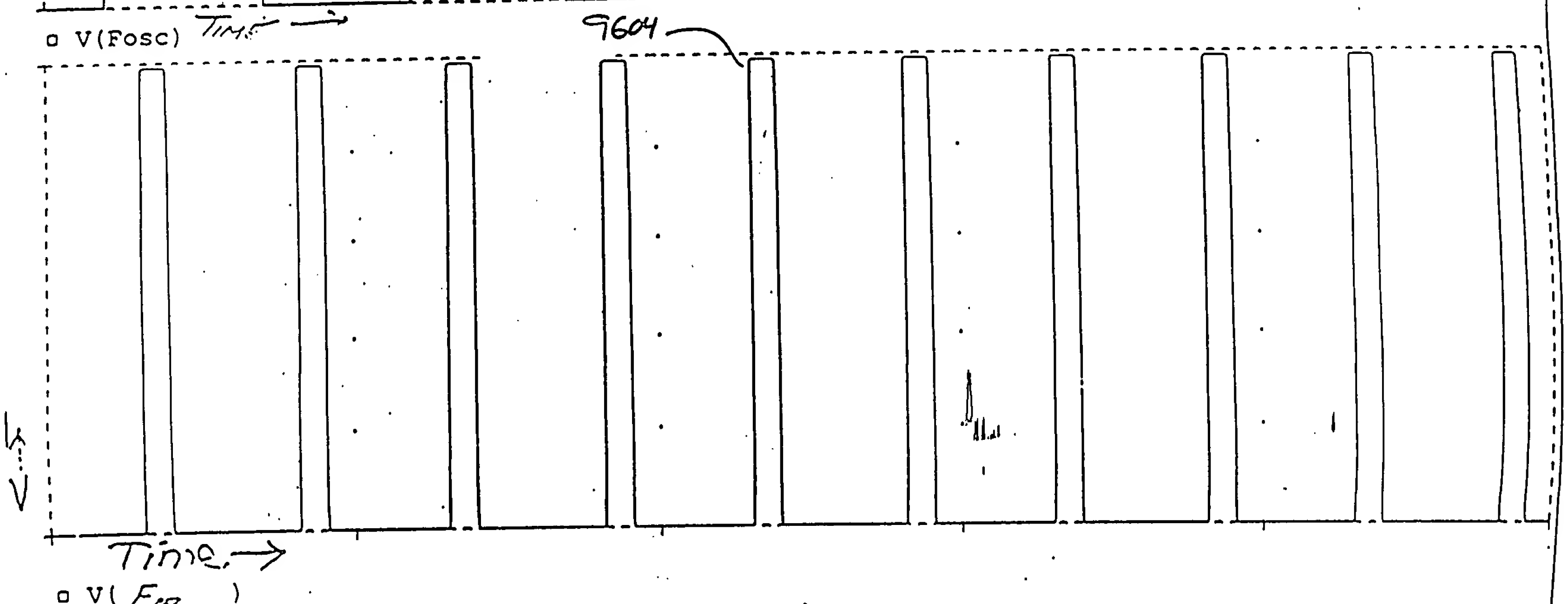


FIG. 96C



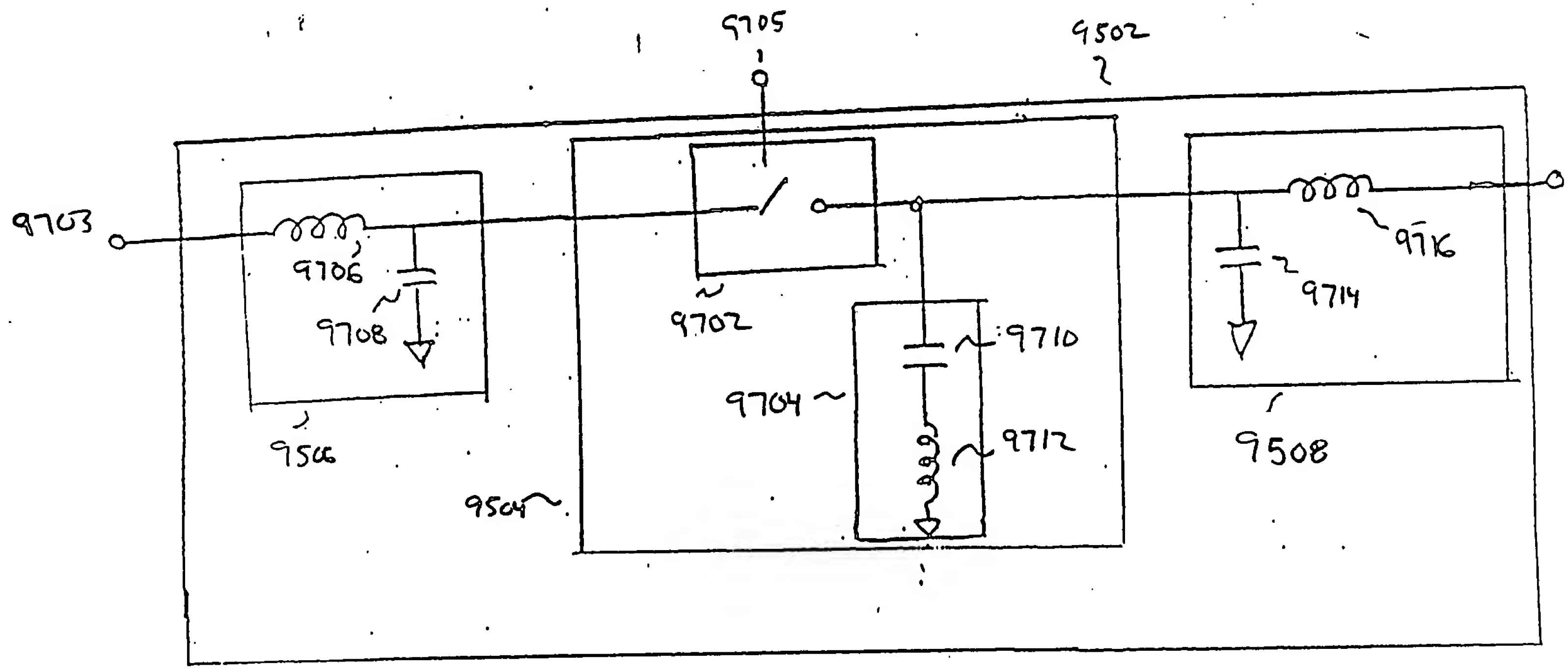


Fig 97 - Aliasing Module

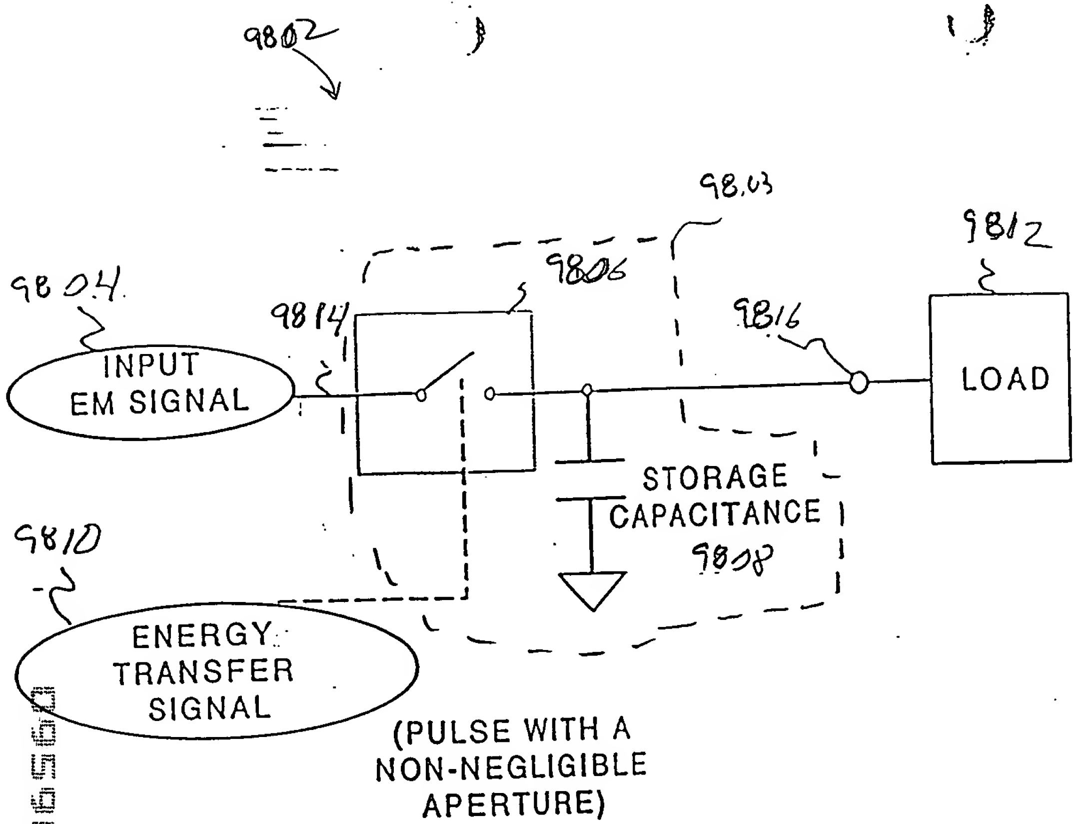


FIG 98A

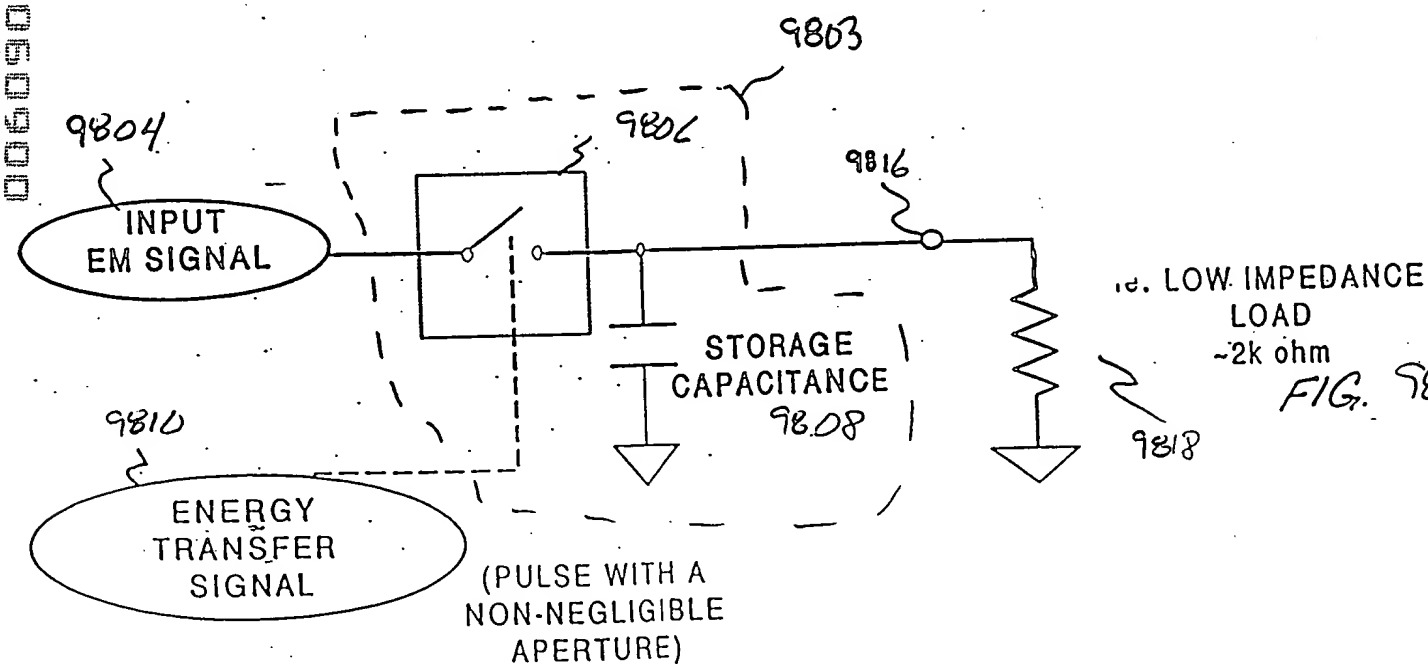


FIG. 98B

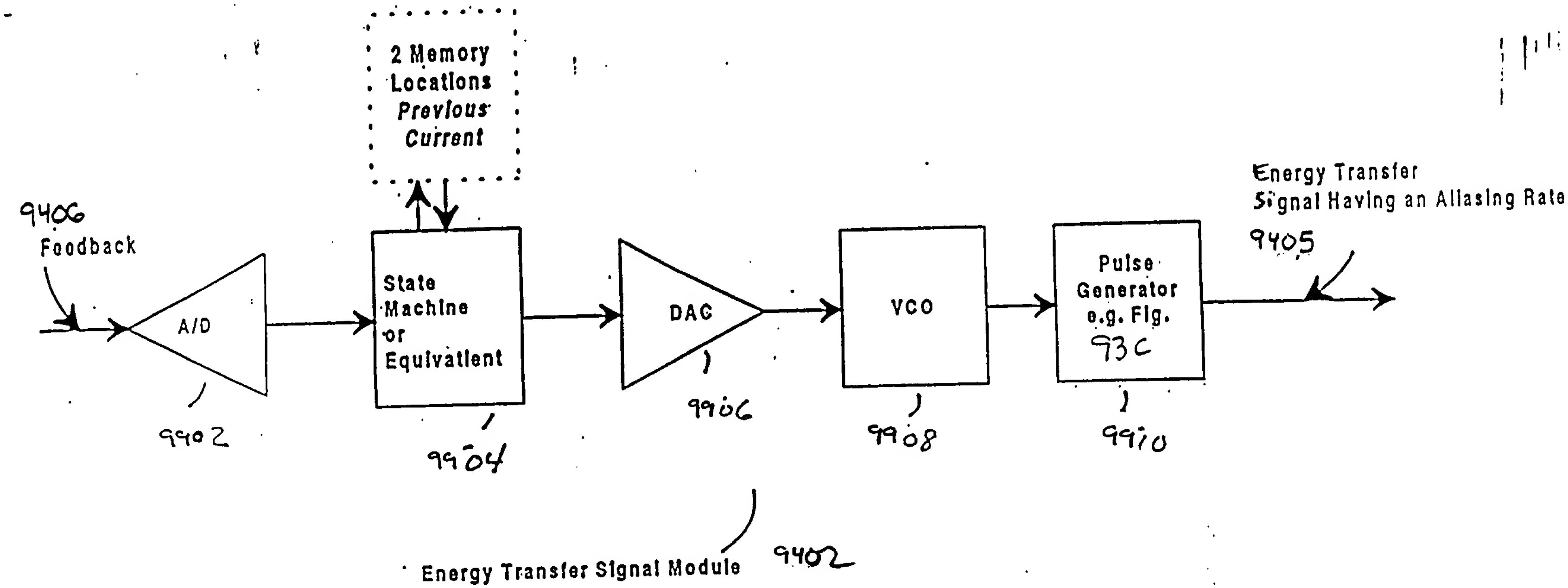
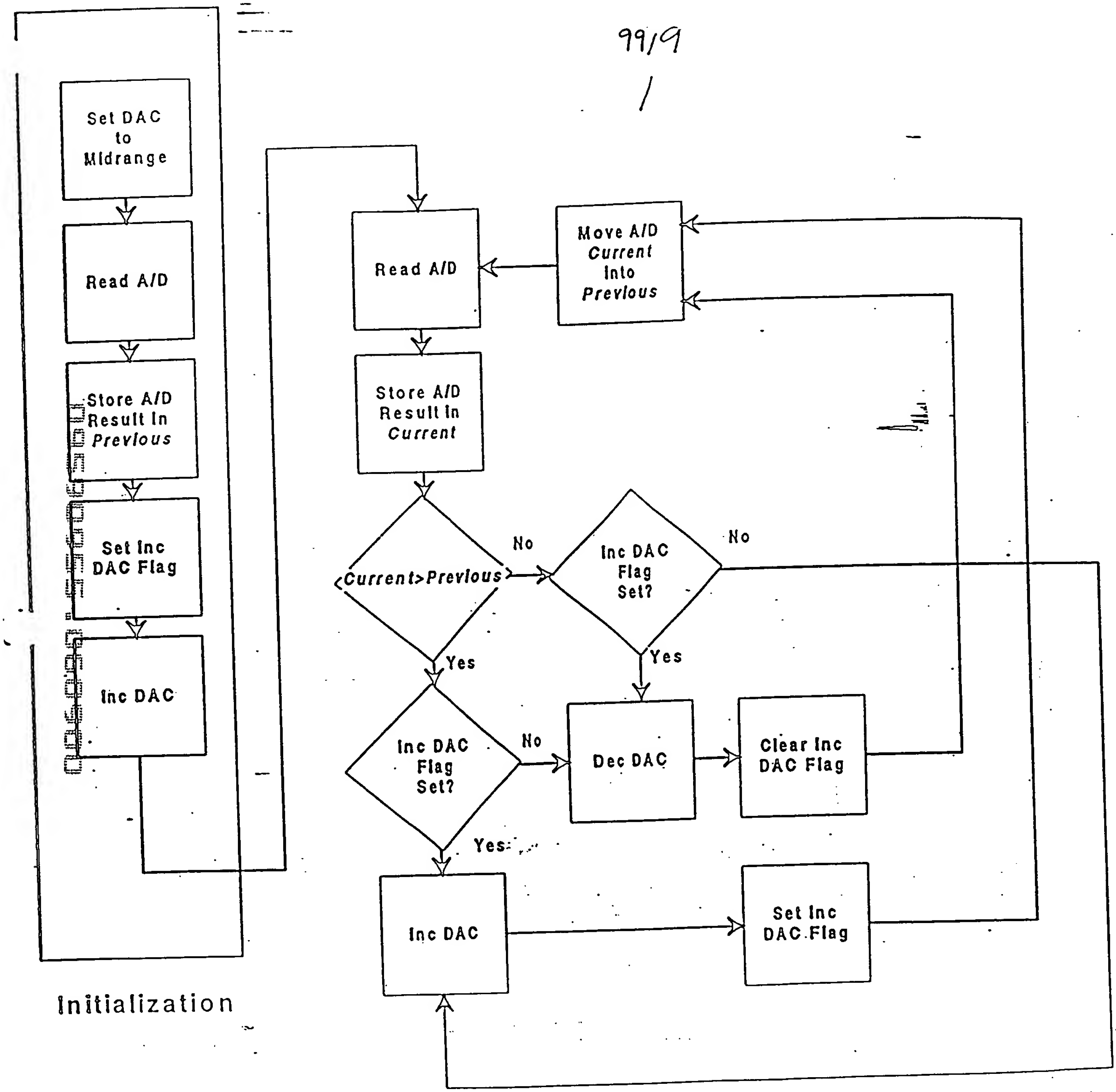

2 Memory
Locations
Previous
Current
9406
Feedback
A/D
9902
State
Machine
or
Equivalent
9904
DAC
9906
VCO
9908
Pulse
Generator
e.g. Fig.
93C
9910
Energy Transfer
Signal Having an Aliasing Rate
9405
Energy Transfer Signal Module
9402

FIG. 99A

99/9



State Machine Flowchart

FIG. 99B

9203

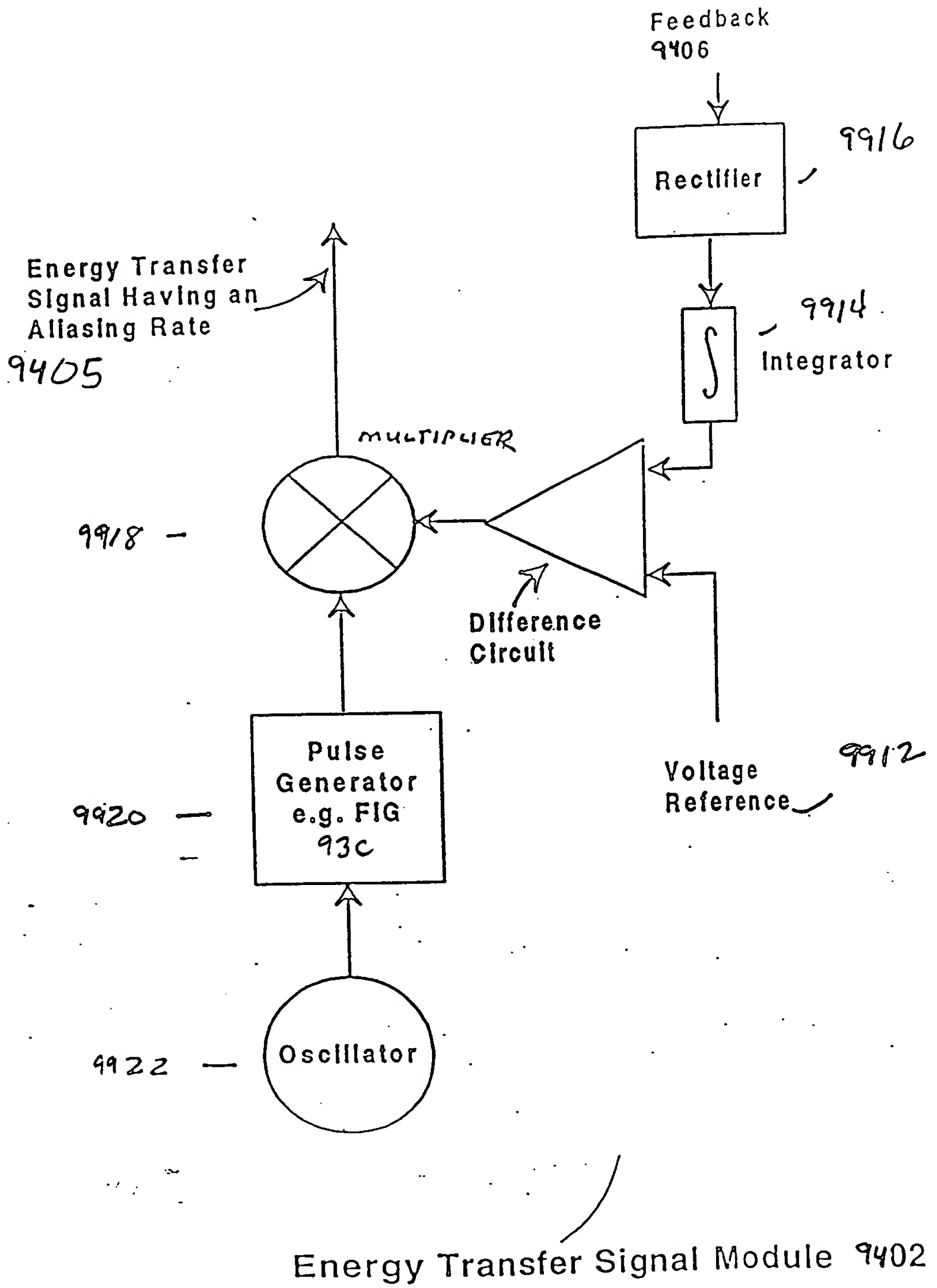

Feedback
9406
Rectifier
9916
9914
Integrator
Energy Transfer Signal Having an Aliasing Rate
9405
MULTIPLIER
9918
Difference Circuit
Pulse Generator e.g. FIG 93c
9920
Voltage Reference
9912
Oscillator
9922
Energy Transfer Signal Module 9402

FIG. 99C

09560655 "090600

5

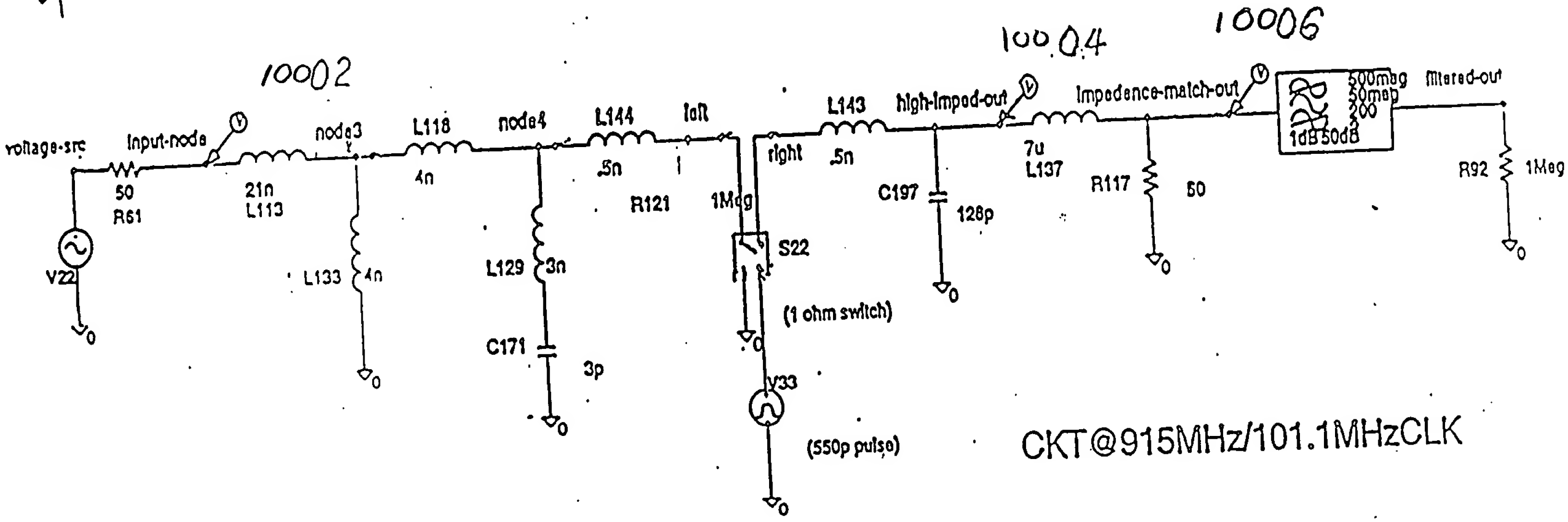
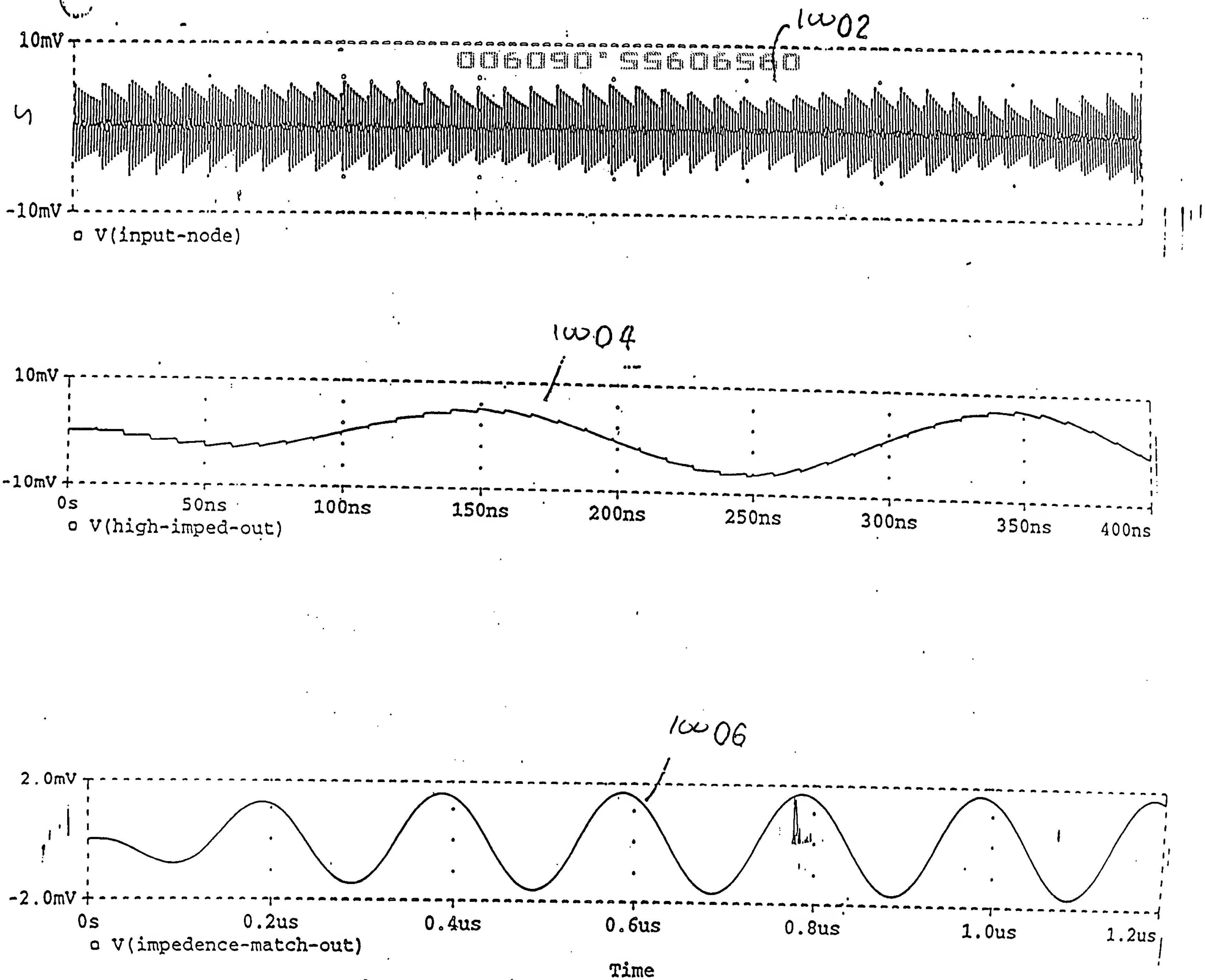


Fig. 100



10mV
-10mV
V(input-node)
10mV
-10mV
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
V(high-imped-out)
2.0mV
-2.0mV
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
V(impedence-match-out)
Time

Fig. 107

10212

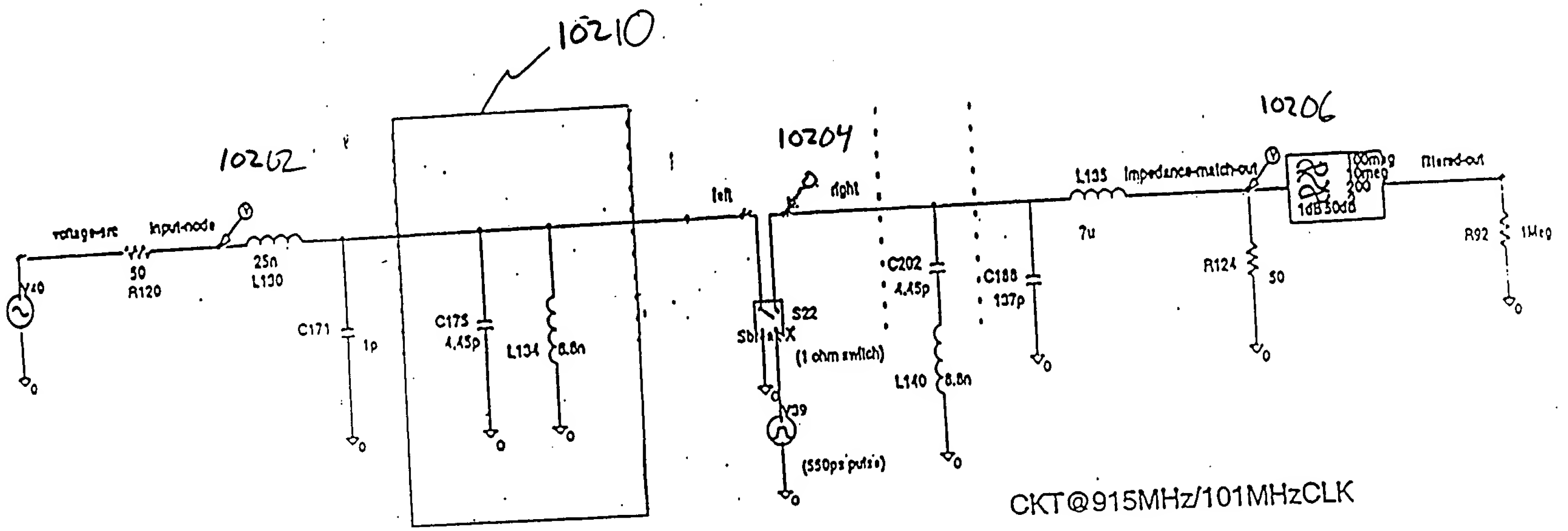


Fig. 102

00609055606560

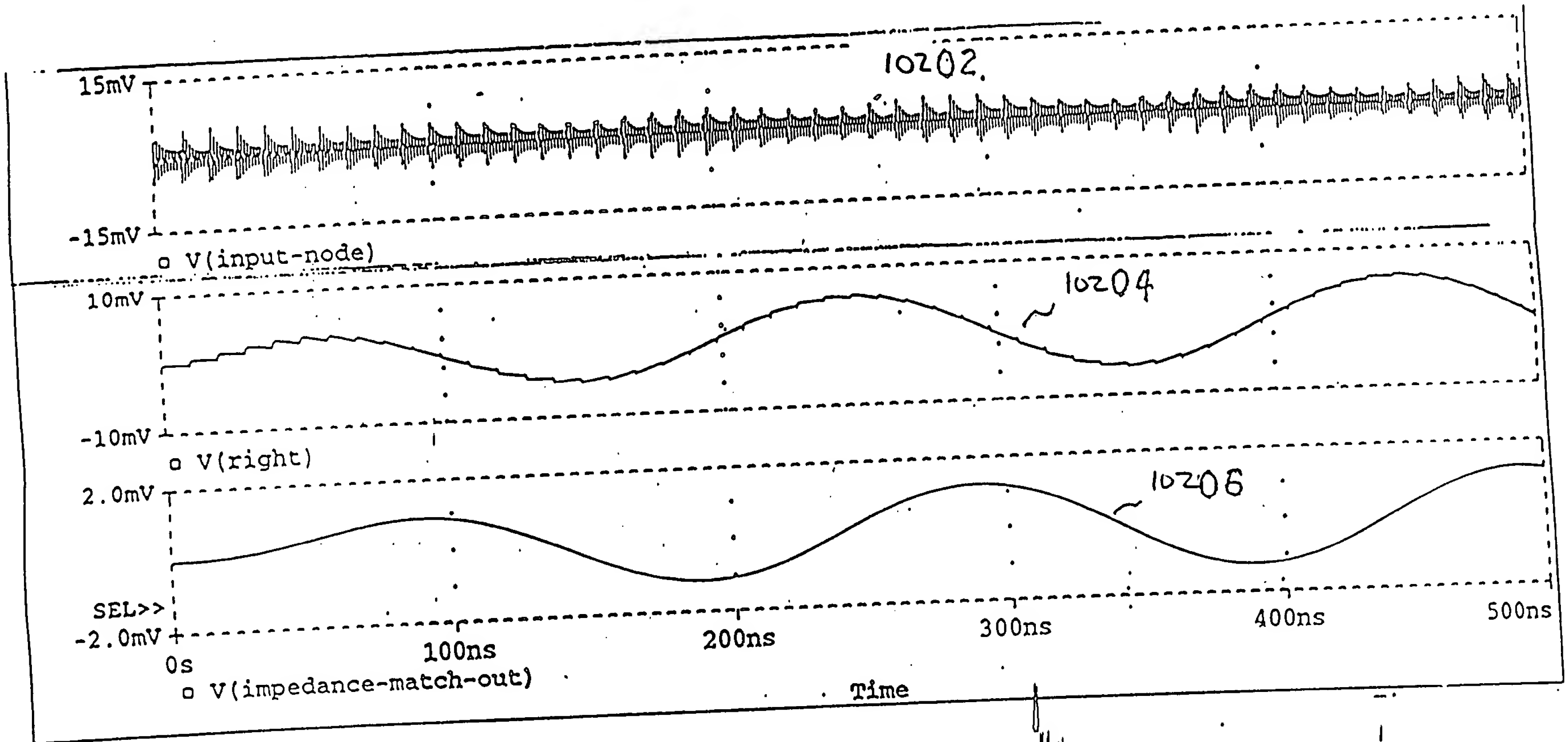


Fig 103

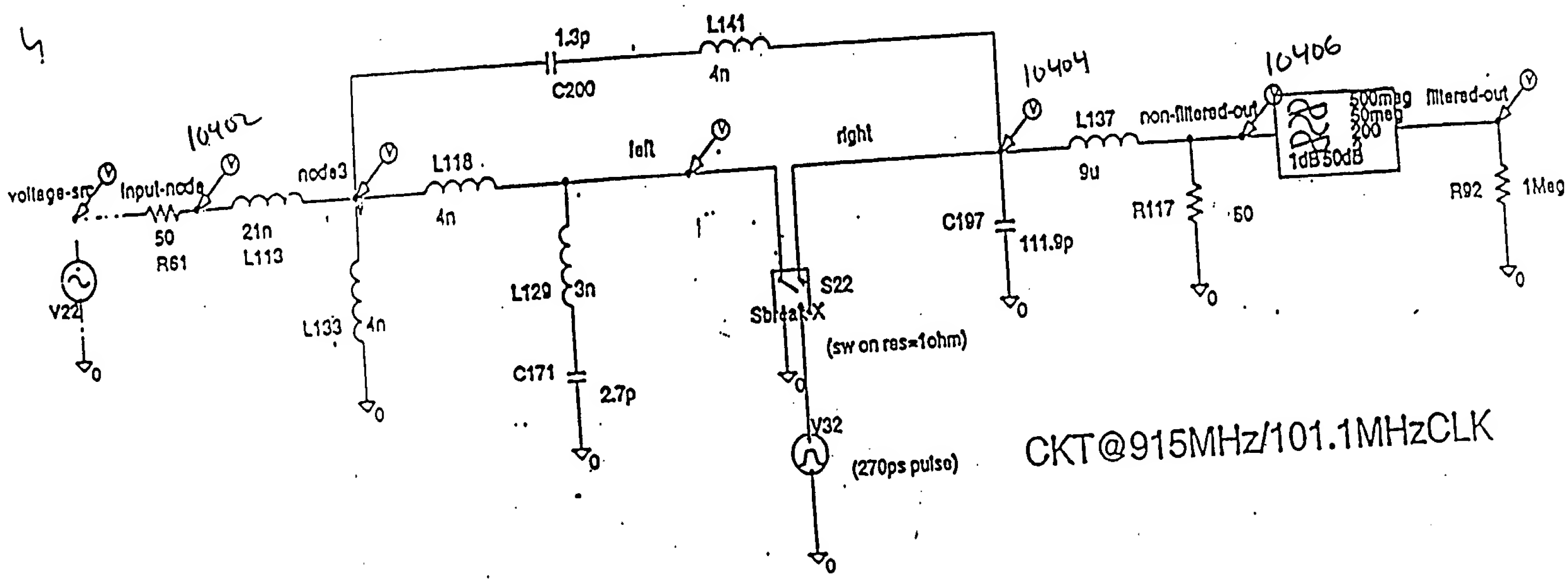

voltage-src
V22
Input-node
50
R61
10402
21n
L113
node3
L133
4n
L118
4n
L129
3n
C171
2.7p
1.3p
C200
L141
4n
left
right
S22
Sbreak X
(sw on res=1ohm)
V32
(270ps pulse)
10404
C197
111.9p
L137
9u
non-filtered-out
R117
50
10406
500meg
50meg
200
1dB 50dB
filtered-out
R92
1Meg
CKT@915MHz/101.1MHzCLK

Fig. 104

006090" 55606560

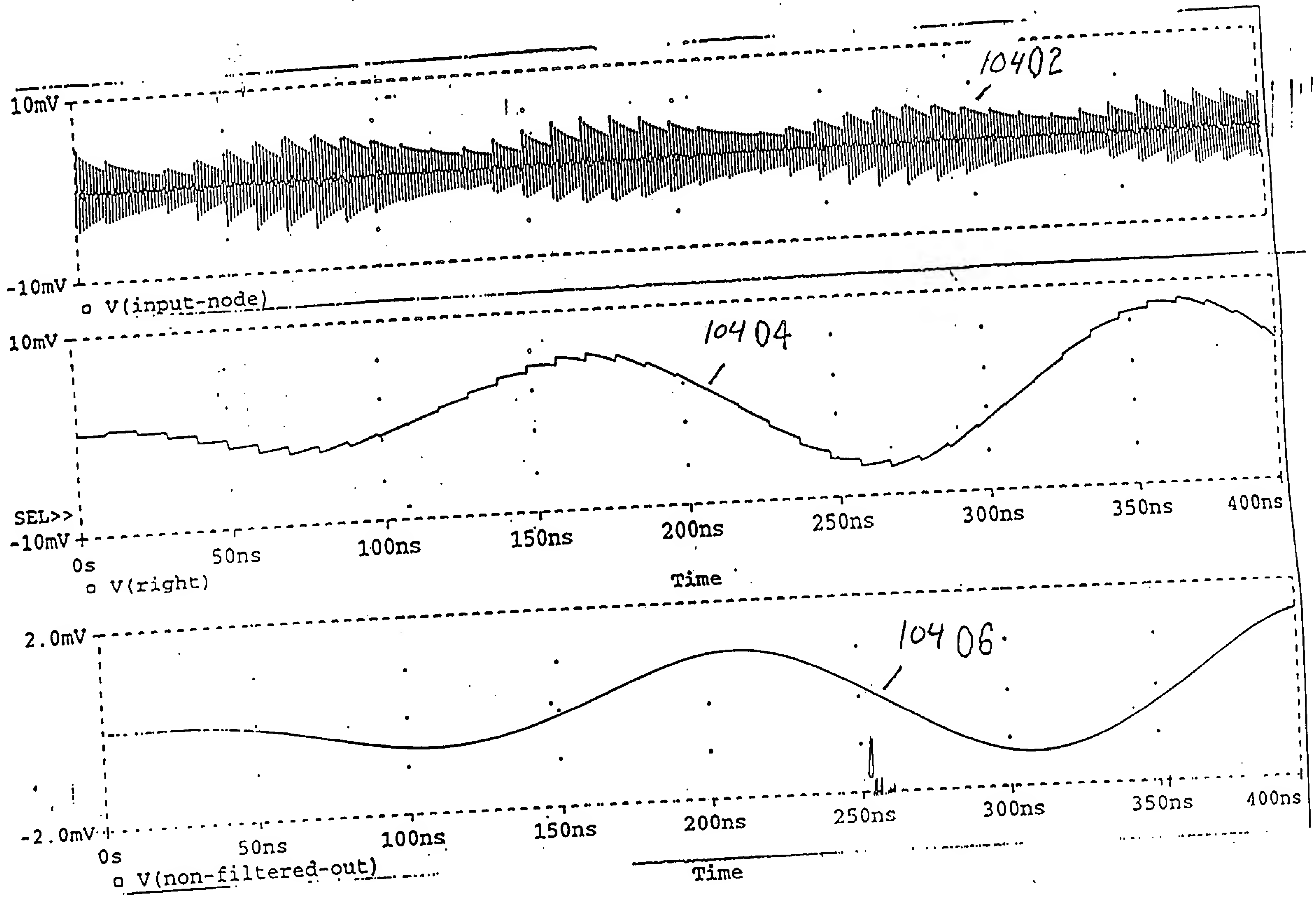


Fig. 105

006090" 55606560

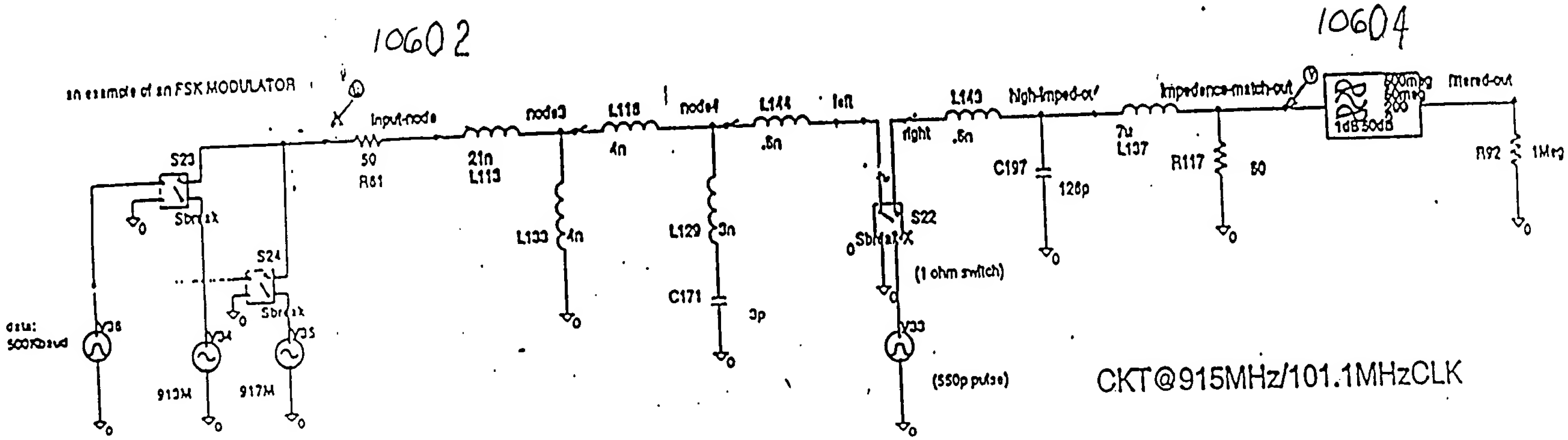
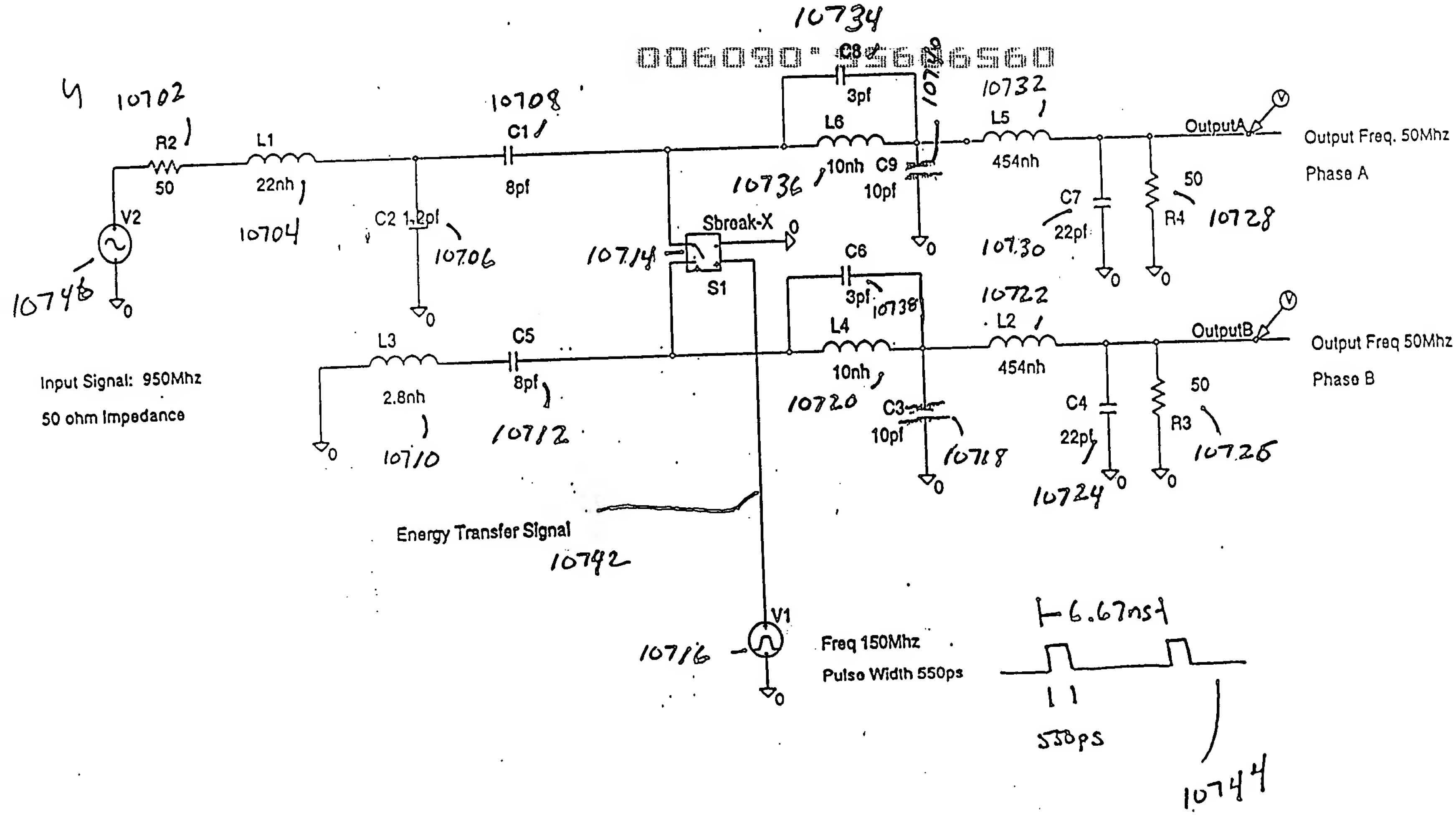


Fig. 106



10702
R2
50
L1
22nh
10704
C2 1.2pf
10706
10708
C1
8pf
10734
C8
3pf
L6
10nh
10736
C9
10pf
10732
L5
454nh
C7
22pf
10730
R4
50
10728
OutputA
Output Freq. 50Mhz
Phase A
V2
10748
Input Signal: 950Mhz
50 ohm Impedance
L3
2.8nh
10710
C5
8pf
10712
Sbreak-X
S1
10714
C6
3pf
10738
L4
10nh
10720
C3
10pf
10718
10722
L2
454nh
C4
22pf
10724
R3
50
10726
OutputB
Output Freq 50Mhz
Phase B
Energy Transfer Signal
10742
V1
10716
Freq 150Mhz
Pulse Width 550ps
6.67ns
550ps
10744

FIG. 107A

* C:\MSim_8\Projects\Wireless\pat1.sch

Temperature: 27.0

006090"55606560

Date/Time run: 10/14/98 15:37:54

(A) pat1.dat

FIG. 107B

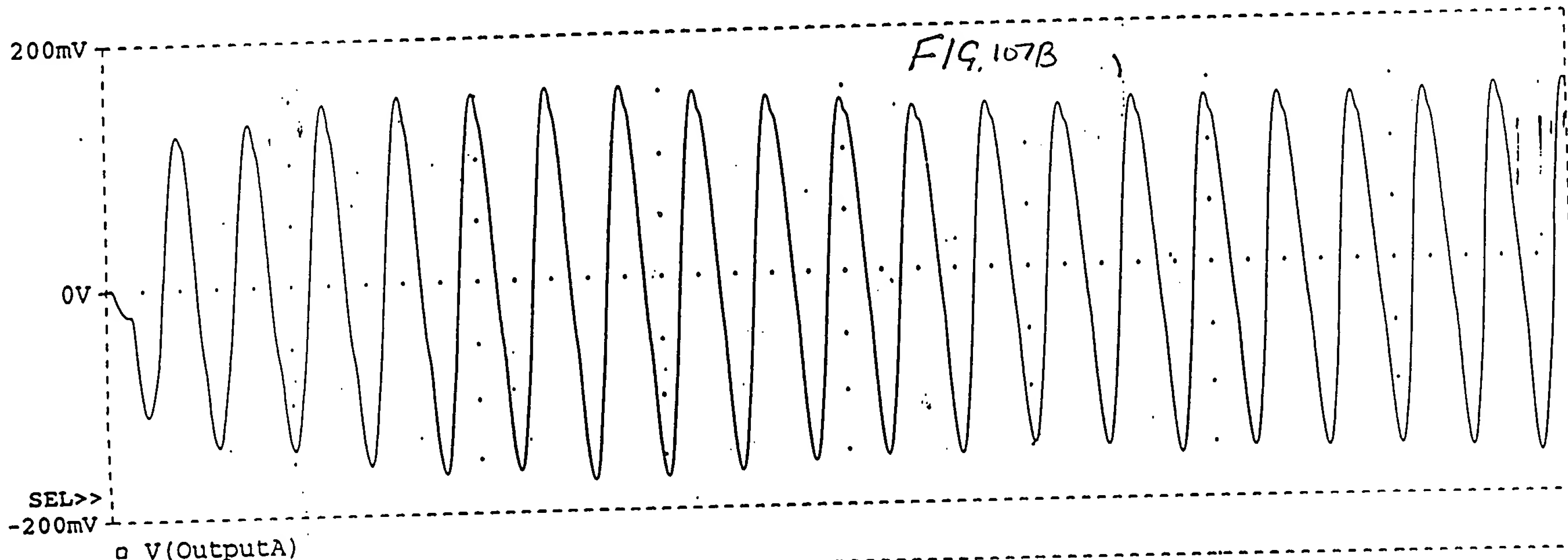
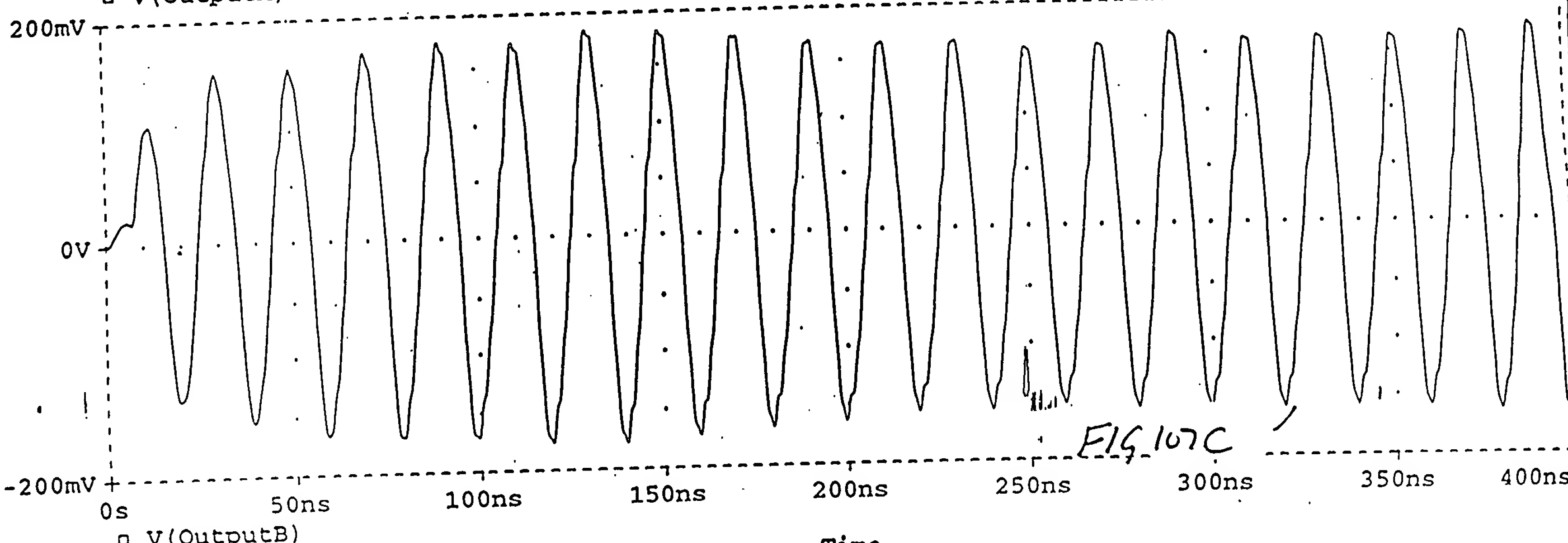


FIG. 107C



Date: October 14, 1998

Page 1

Time: 15:41:42

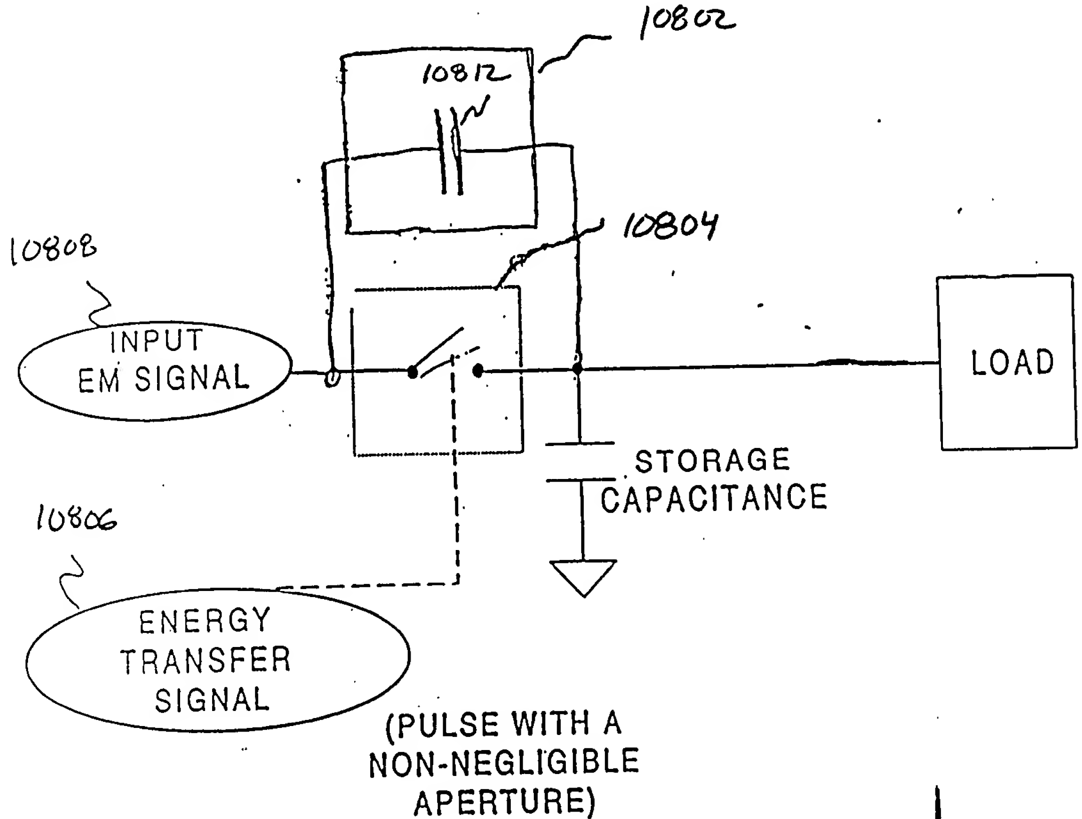
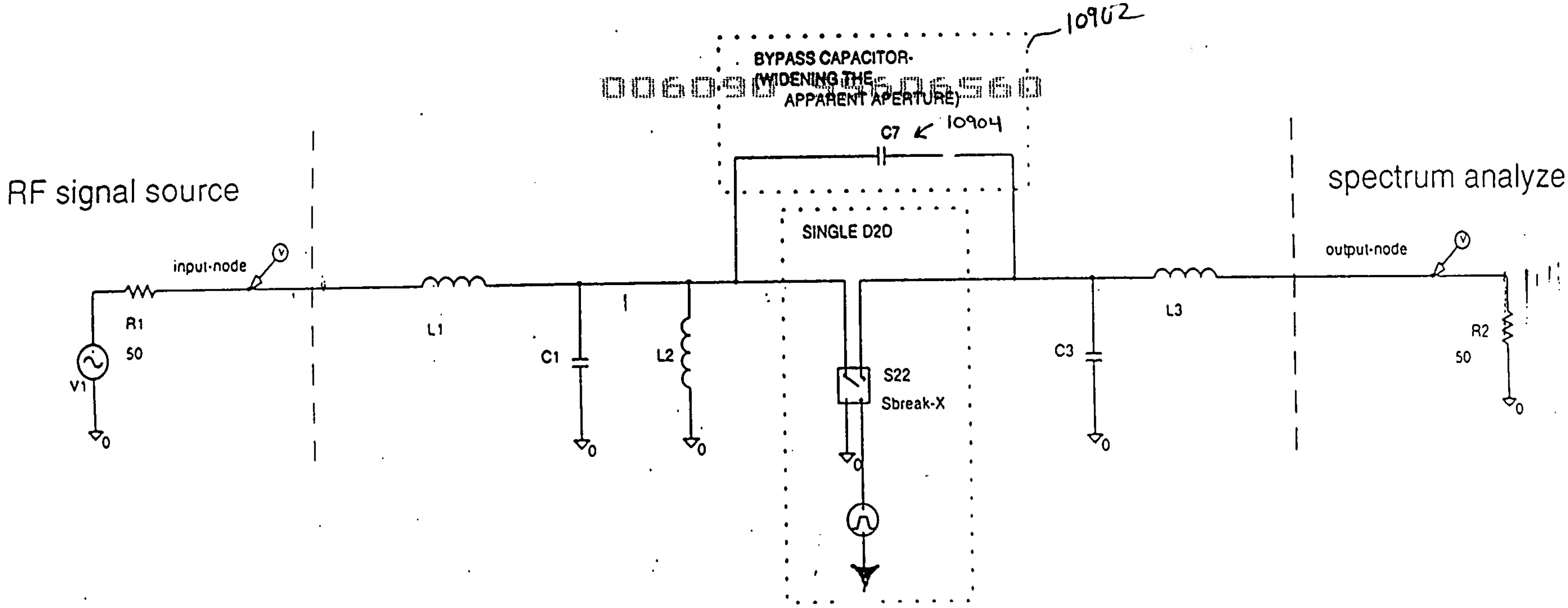

10802
10812
10804
10808
INPUT
EM SIGNAL
LOAD
STORAGE
CAPACITANCE
10806
ENERGY
TRANSFER
SIGNAL
(PULSE WITH A
NON-NEGLIGIBLE
APERTURE)

Fig. 108



10902
BYPASS CAPACITOR-
(WIDENING THE
APPARENT APERTURE)
C7
10904
RF signal source
spectrum analyzer
SINGLE D2D
input-node
output-node
R1
50
V1
L1
C1
L2
S22
Sbreak-X
C3
L3
R2
50

FIG. 109

006090" SS606560

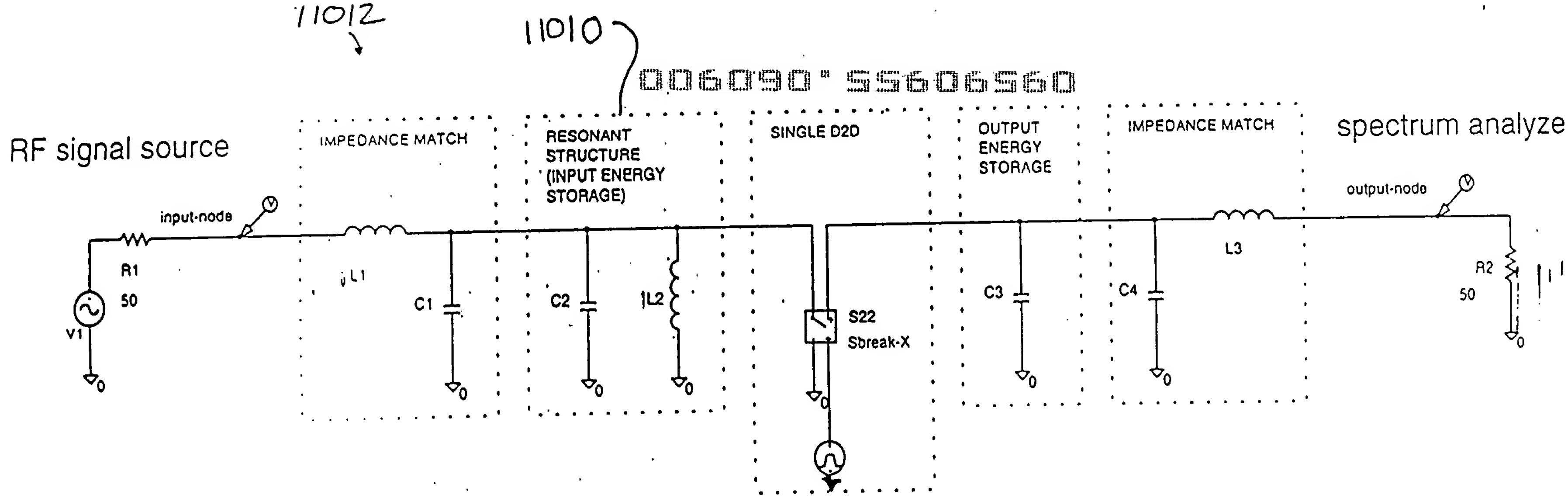


FIG. 110

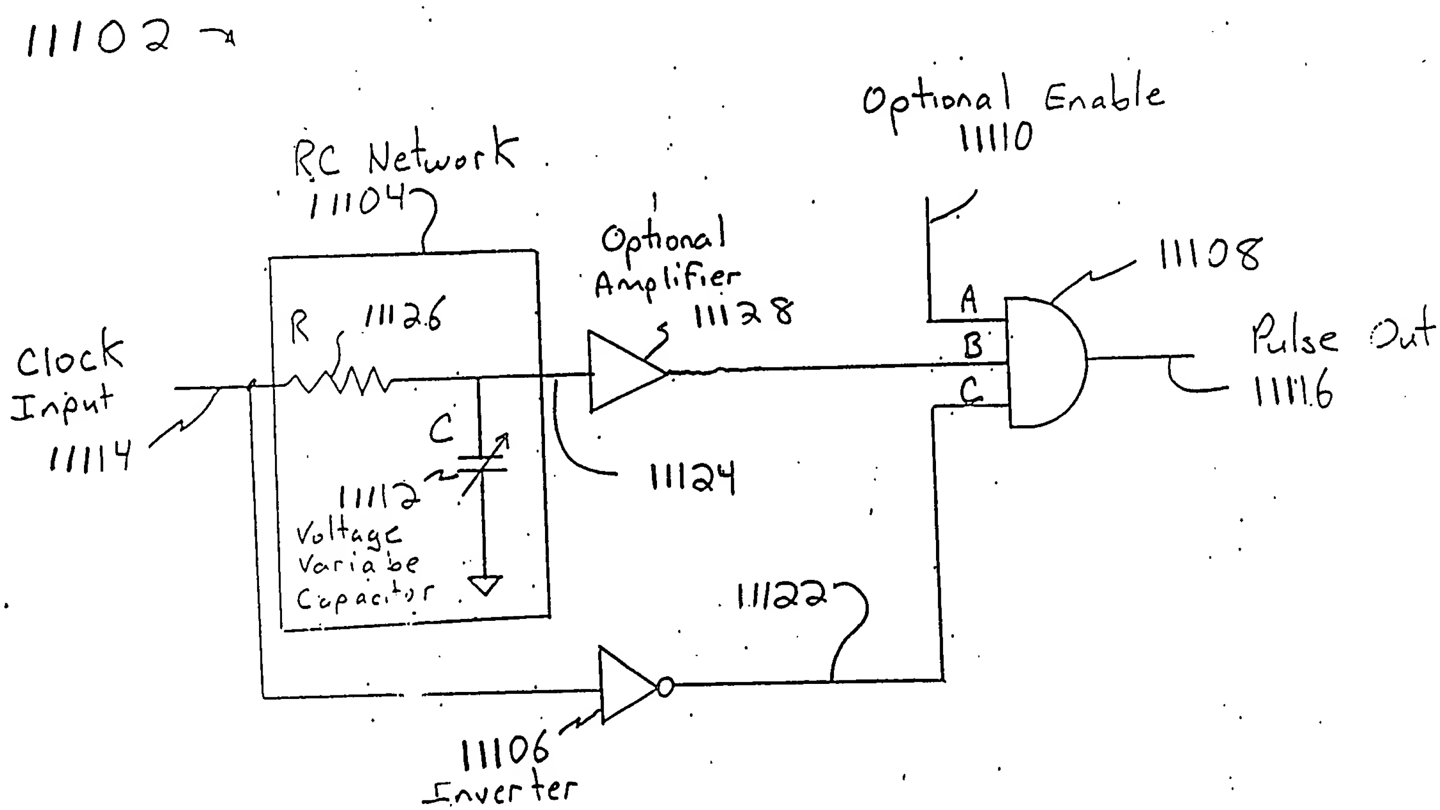

11102
Optional Enable
11110
RC Network
11104
Optional
Amplifier
11128
11108
A
B
C
Pulse Out
11116
R
11126
Clock
Input
11114
C
11112
Voltage
Variabe
Capacitor
11124
11122
11106
Inverter

FIG. 111A

006090" SS606560

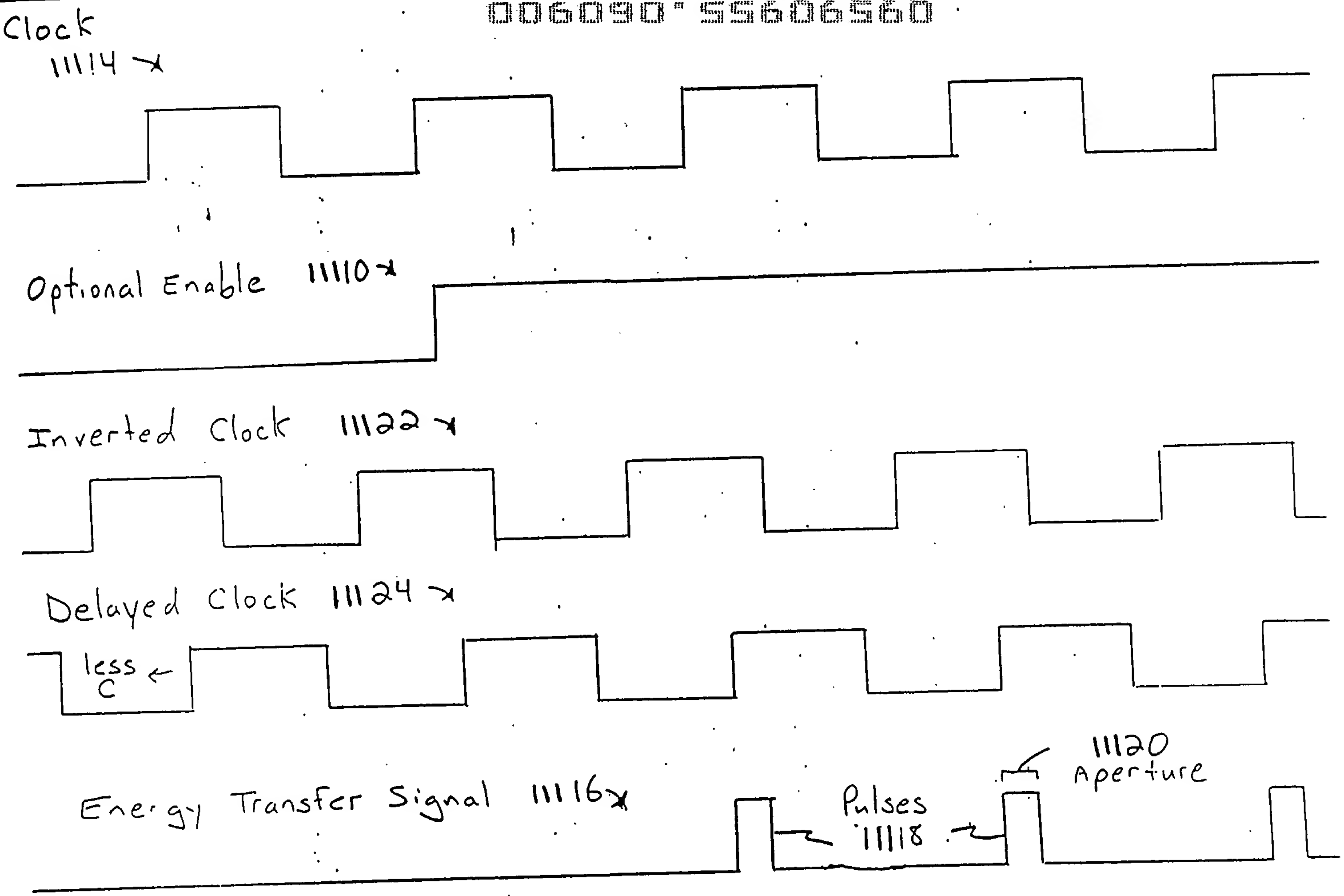


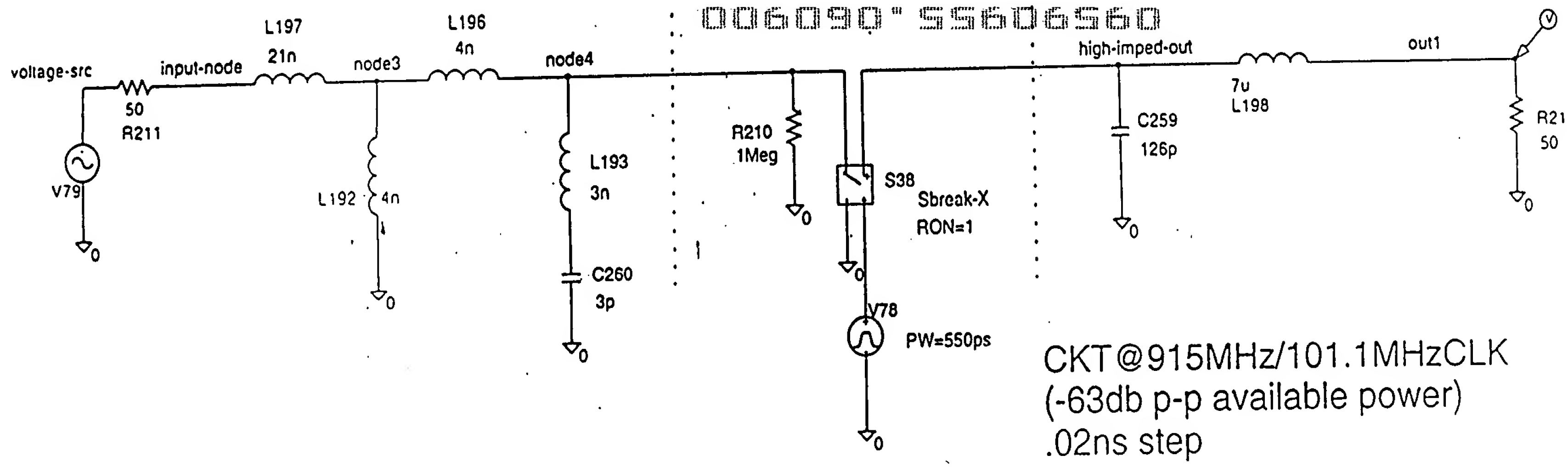
FIG 111B

FIG 111C

FIG 111D

FIG 111E

FIG 111F

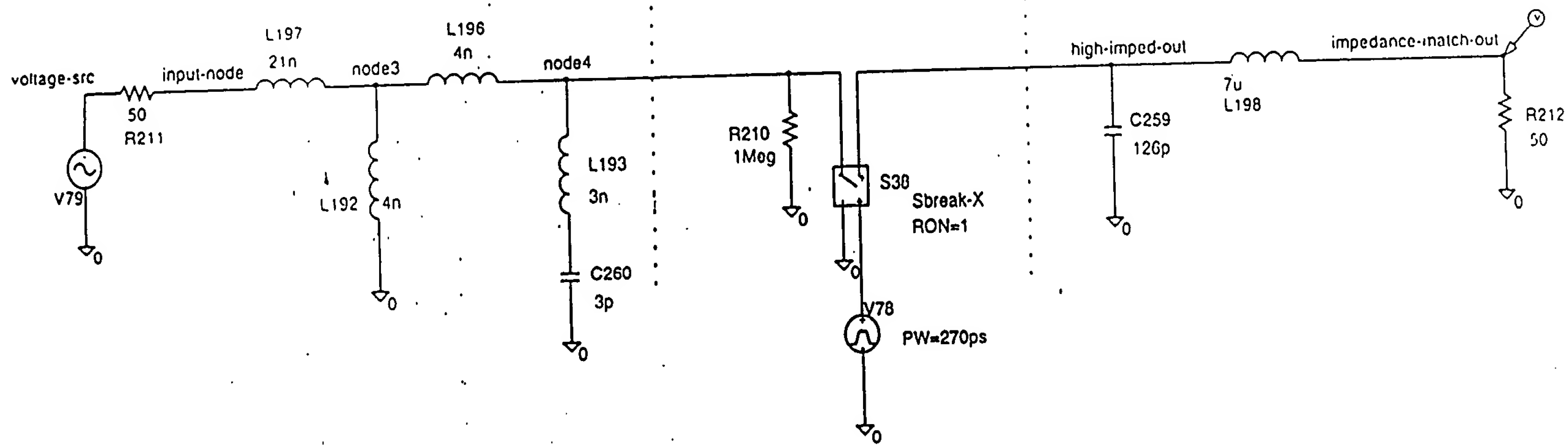


CKT@915MHz/101.1MHzCLK
(-63db p-p available power)
.02ns step

single-series-switch-915M-5M-hieff.sch

FIG. 1/12

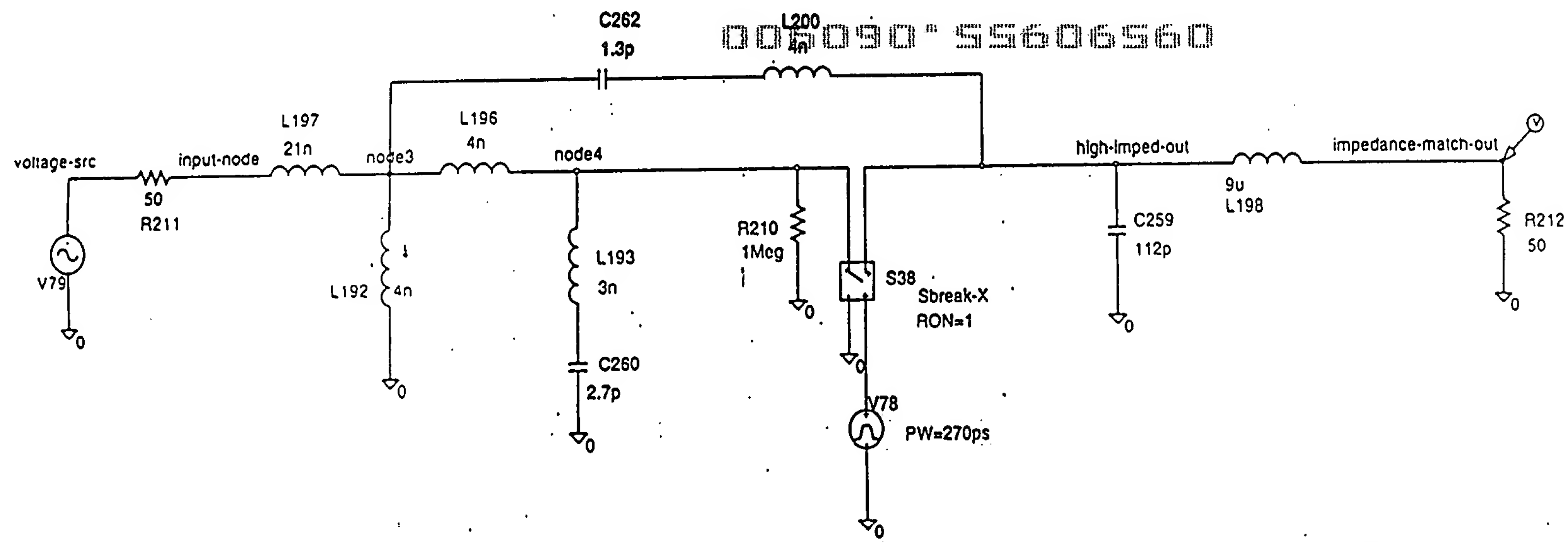
00609055 . 090600



CKT@915MHz/101.1MHzCLK
(-63db p-p available power)
.02ns step

single-series-switch-smaperture915M-5M-hieff.sch

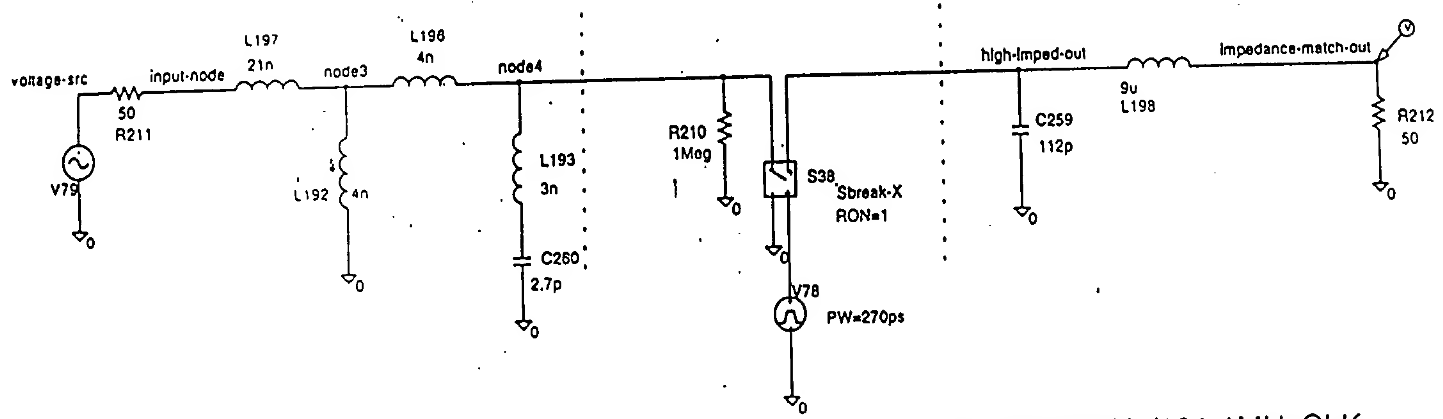
FIG. 113



CKT@915MHz/101.1MHzCLK
(-63db p-p available power)
.02ns step

single-series-switch-bypass-915M-5M-hieff.sch

FIG 114



CKT@915MHz/101.1MHzCLK
(-63db p-p available power)
.02ns step

single-series-switch-wobypass-915M-5M-hieff.sch

FIG. 115

(E) single-series-switch-915M-5M-hieff.dat

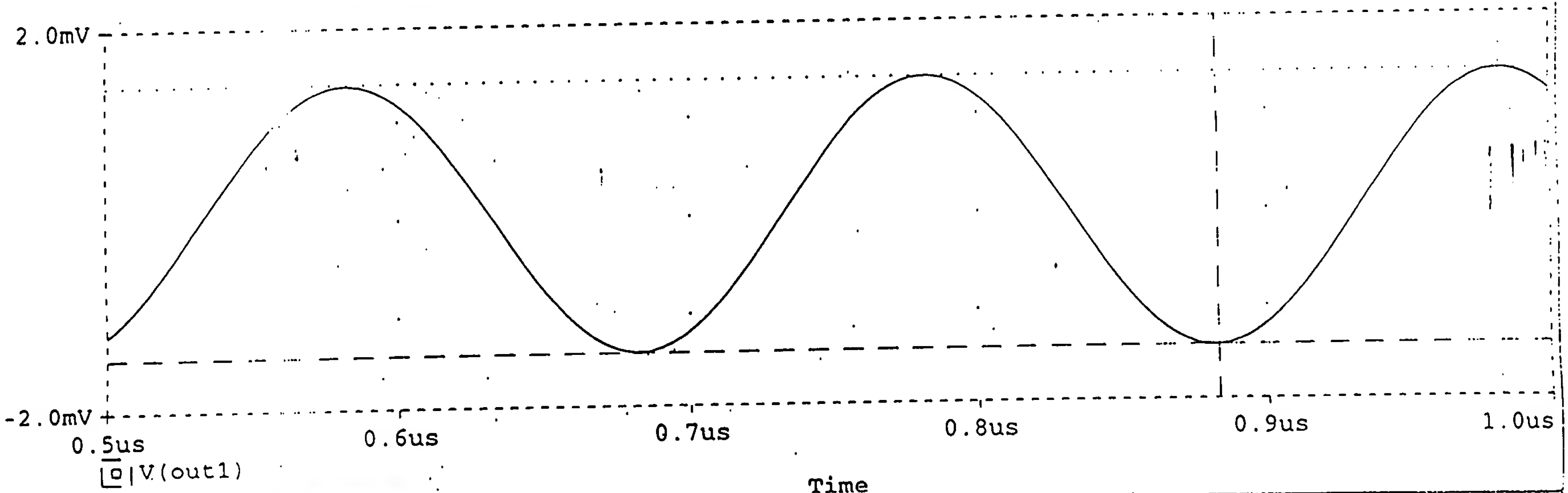


FIG. 116A

(F) single-series-switch-smaperture915M-5M-hieff.dat

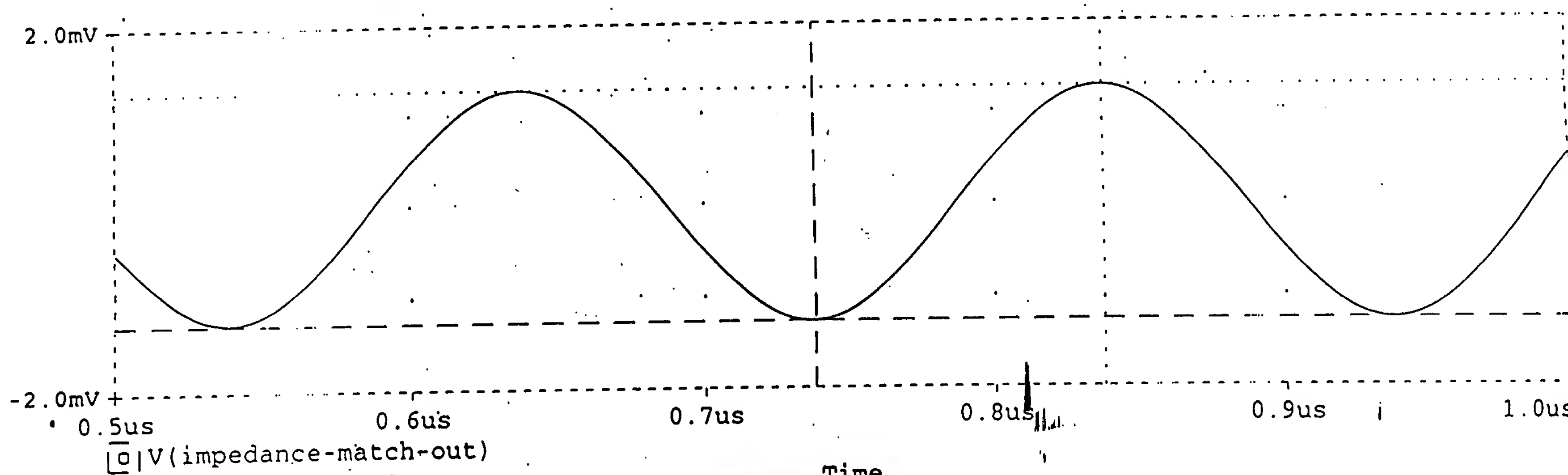


FIG. 116B

E1:(981.86n,1.404m) E2:(883.04n,-1.402m) DIFF(E):(98.82n,2.806m)
F1:(837.43n,1.253m) F2:(738.01n,-1.252m) DIFF(F):(99.42n,2.505m)

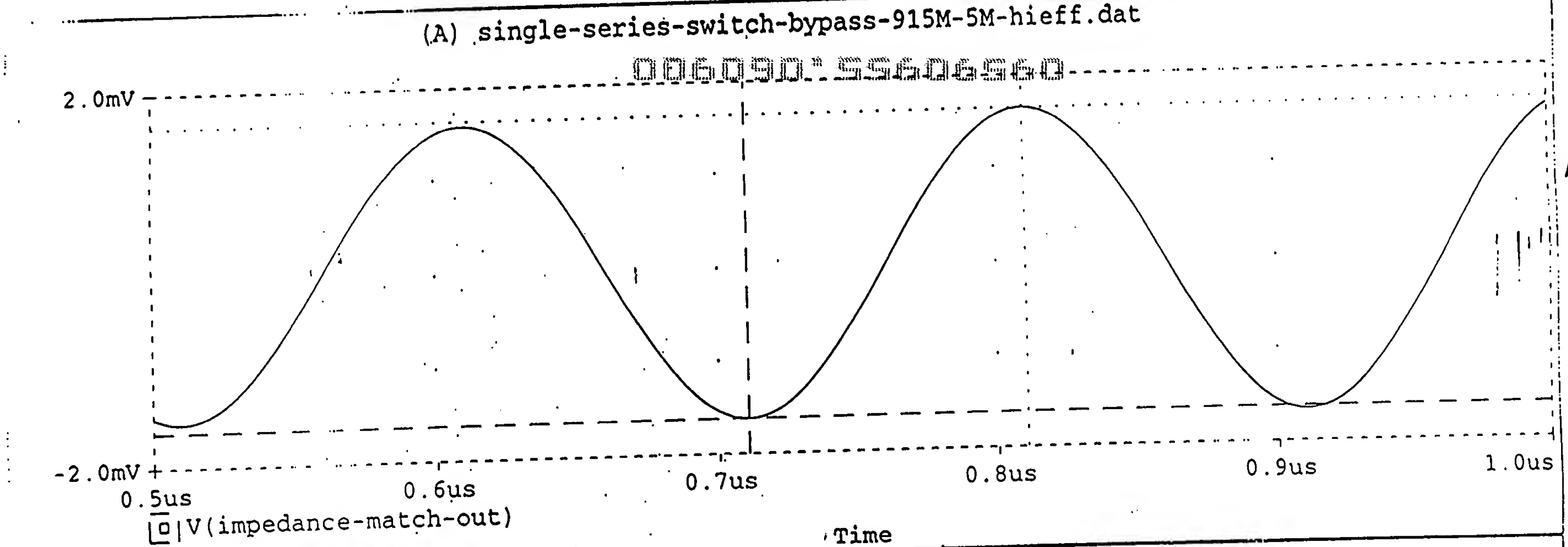


FIG. 117A

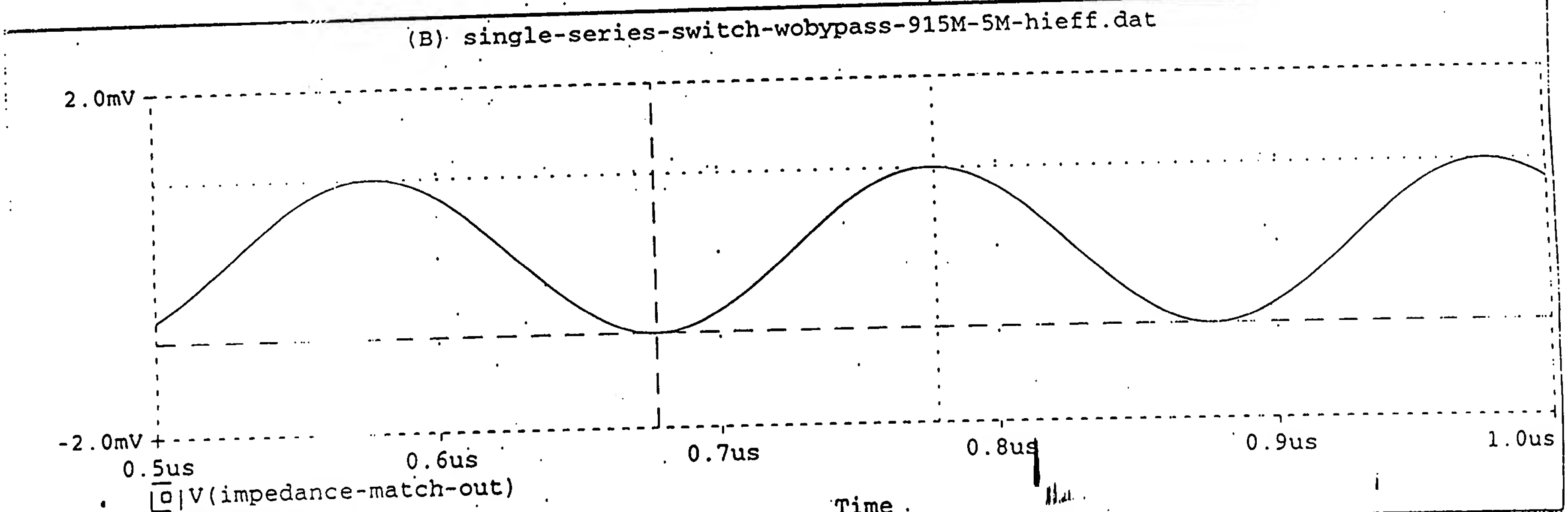


FIG. 117B

A1:(810.53n,1.642m) A2:(710.52n,-1.621m) DIFF(A):(100.01n,3.263m)
B1:(777.78n,942.32u) B2:(677.18n,-942.51u) DIFF(B):(100.60n,1.885m)

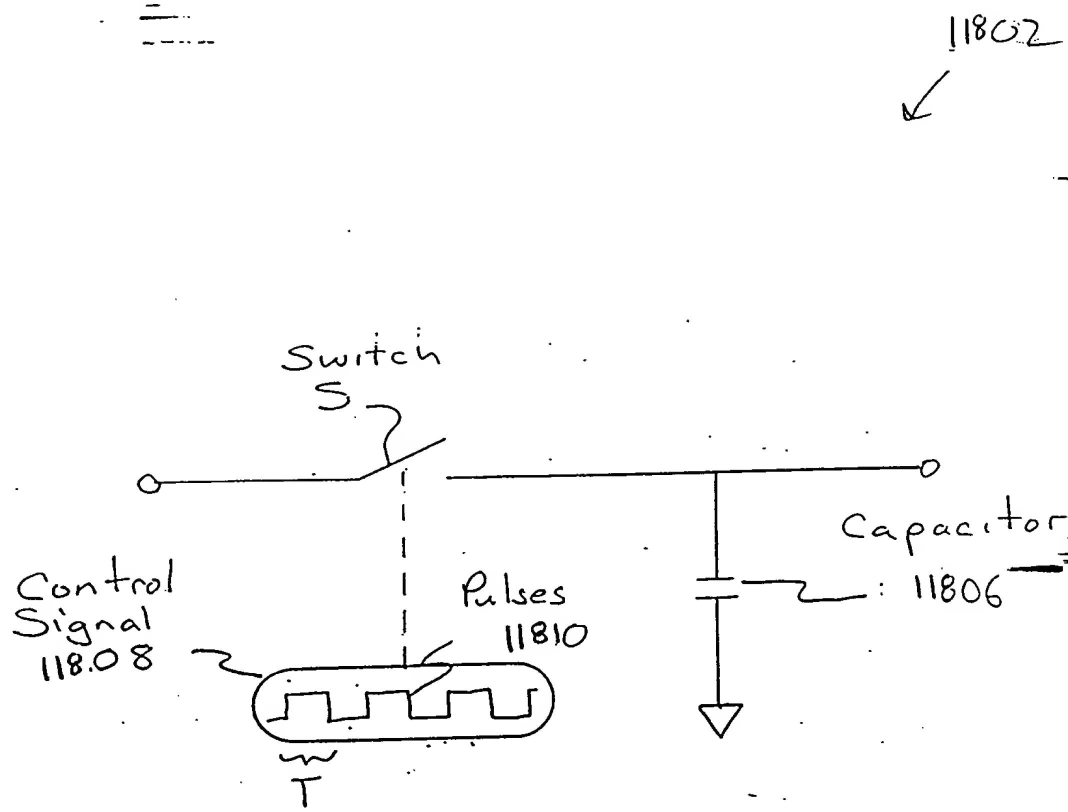

11802
Switch
S
Capacitor
11806
Control
Signal
118.08
Pulses
11810
T

FIG. 118A

$$q=C\cdot V$$ EQ. A

$$V=A\cdot \sin(t)$$ EQ. B

$$q(t)=C\cdot A\cdot \sin(t)$$ EQ. C

$$\Delta q(t)=C\cdot A\cdot \sin(t)-C\cdot A\cdot \sin(t-T)$$ EQ. D

$$\Delta q(t)=C\cdot A\cdot (\sin(t)-\sin(t-T))$$ EQ. E

$$\sin(\alpha)-\sin(\beta)=2\cdot \sin\left(\frac{\alpha-\beta}{2}\right)\cdot \cos\left(\frac{\alpha+\beta}{2}\right)$$ EQ. F.

$$\Delta q(t)=2\cdot C\cdot A\cdot \sin\left[\frac{t-(t-T)}{2}\right]\cdot \cos\left[\frac{t+(t-T)}{2}\right]$$ EQ. G

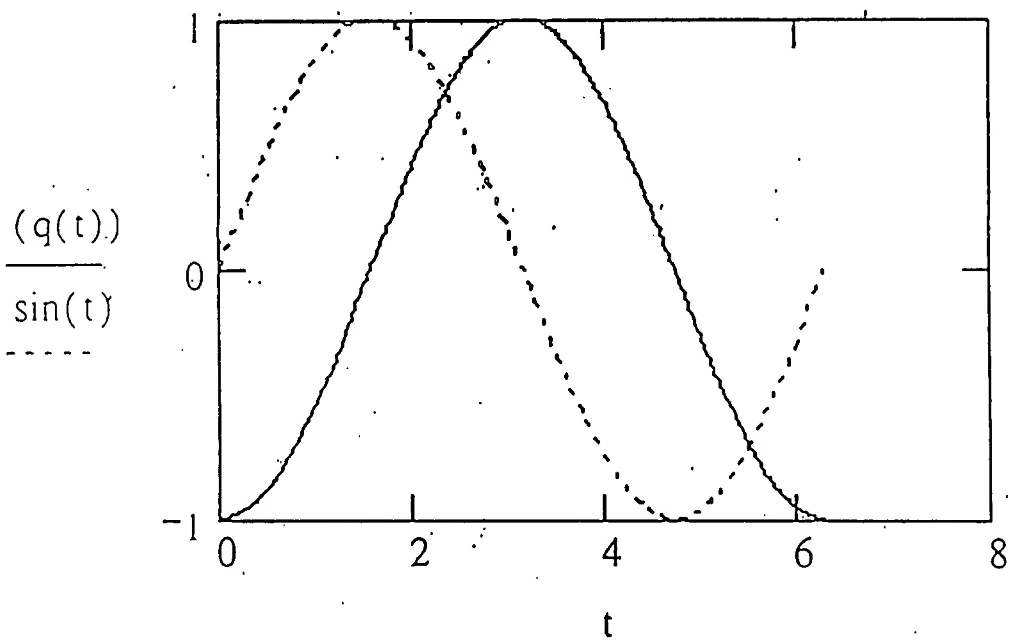
$$\Delta q(t)=2\cdot C\cdot A\cdot \sin\left(\frac{1}{2}\cdot T\right)\cdot \cos\left(t-\frac{1}{2}\cdot T\right)$$ EQ. H

$$q(t)=\int C\cdot A\cdot (\sin(t)-\sin(t-T))\,dt$$ EQ. I

$$q(t)=-\cos(t)\cdot C\cdot A+\cos(t-T)\cdot C\cdot A$$ EQ. J

$$q(t)=C\cdot A\cdot (\cos(t-T)-\cos(t))$$ EQ. K

FIG. 110B

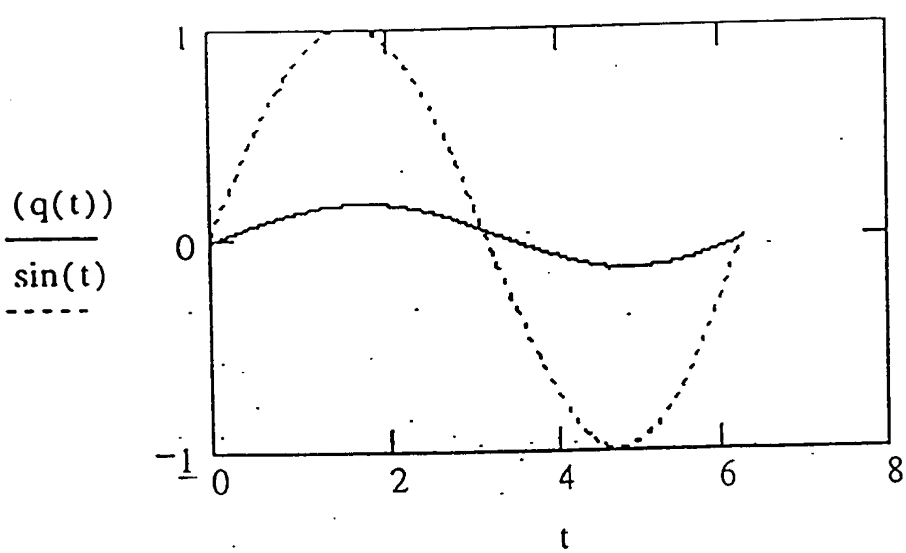


Graph 1

C=1;A=.5,T=¶

FIG. 118C

For Graph 2: C=1, A=.5, T=π/10:



Graph 2

FIG 118D

Power - Charge Relationship

$$q = C \cdot V$$ EQ. L

$$V = \frac{q}{C}$$ EQ. M

$$V = \frac{J}{C}$$ EQ. N

$$J = \frac{q^2}{C}$$ EQ. O

$$P = \frac{J}{S}$$ EQ. P

$$P = \frac{q^2}{C \cdot S}$$ EQ. Q

FIG. 118E

Insertion Loss

Insertion loss in dB is expressed by:

$$ILdB = 10 \cdot \log\left(\frac{Pin}{Pout}\right)$$

or

$$ILdB = 10 \cdot \log\left[\frac{\left(\frac{Vin^2}{Rin}\right)}{\left(\frac{Vout^2}{Rout}\right)}\right]$$

FIG. 118F

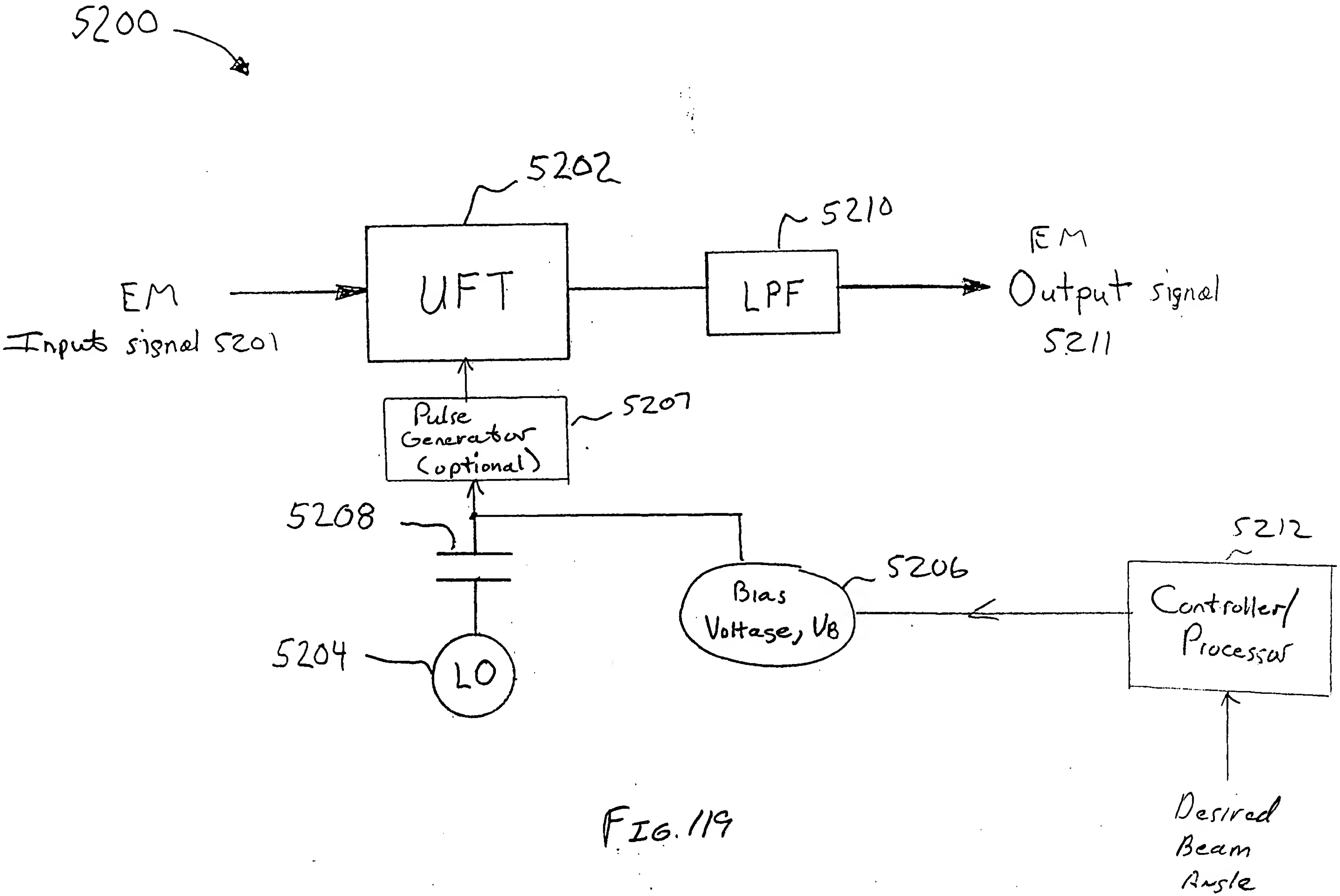

5200
EM
Inputs signal 5201
UFT
5202
LPF
5210
EM
Output signal
5211
Pulse
Generator
(optional)
5207
5208
5204
LO
Bias
Voltage, V_B
5206
Controller/
Processor
5212
Desired
Beam
Angle

FIG. 119